Soft Error Filtered and Hardened Latch

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Abstract — *this paper presents a low-power soft error-hardened latch suitable for reliable circuits. The proposed circuit uses redundant feedback loop to protect latch circuit against soft error on the internal nodes and skewed CMOS to filter out transients resulting from particle hit on combinational logic. The proposed circuit has low power consumption, enhanced setup time and lower timing overhead. The HSPICE post-layout simulations in 90nm CMOS technology reveals that circuit is able to recover from single particle strike on internal nodes and tolerates input SETs up to 130ps of duration†.*

Index Terms — soft-error, reliability, latch, skewed CMOS.

I. INTRODUCTION

The smaller node capacitance due to aggressive device dimensions shrinkage along with the power supply voltage reduction, leads to smaller amount of stored charge on each circuit node. This smaller stored charge and higher operating frequency now make CMOS circuits more vulnerable to soft errors caused by charge deposited directly by alpha particle or indirectly by cosmic ray neutrons [1]. The soft errors which were traditionally regarded as reliability issue for space applications are going to be a terrestrial issue.

Particle hit with lower energy occur far more frequently than particles with higher energy [1]. So as CMOS device sizes and critical charge value decreases, it is more probable that circuit becomes affected by even lower energy particles, potentially leading to higher soft error rate.

Although package and process engineering may reduce alpha particle problem, there is no physical obstacle to cosmic neutrons. Thus improved circuit design methodologies to reduce soft error vulnerability are becoming mainstream approach for high reliability systems.

With advanced sub-micron technology, latches and flip-flops are becoming more susceptible to particle strike from two sources: the particle stroke external logic and storage element captures resulted transient, or particle may hit on internal nodes of storage elements.

Due to increased suitability and higher demanded reliability, more hardening and protection on logic and storage elements is required. Most common circuit level protection methods are based on temporal and spatial redundancy. Those methods, as well as scan based SER resilient latch [16] and RAZOR I flip-flop and transient detection of Razor II flip-flop [14] are not able to tolerate single event transient due to particle hit on combinational logic. On the other hand, the temporal redundancy based latches as well as those based on Schmitt-trigger [11] and transmission gate noise filtering effects [13] has extended setup time problem, which leads to performance penalty. The contribution of this work is to propose a circuit which uses noise filtering and redundancy simultaneously to reduce SEU and SET susceptibility with less timing overhead.

The rest of this paper is organized as follows. In section II, the previous works will be reviewed quickly. Section III proposes the SER-tolerant latch. Section IV gives simulation results and section V concludes the paper.

II. LATCH-HARDENING METHODS

In this section, starting with some basic definitions recent publication on latch hardening methods will be reviewed. Generally a particle may hit logic gates, storage elements, or clock network of a digital circuit. When it hits the drain of transistors in logic gates, injects charge and causes a glitch in the output node voltage which is called single event transient (SET) [1][2]. When a particle hits an internal node of a storage element, i.e., latch or flip-flop, it may change stored data and cause single event upset (SEU). Also SET may generate and propagate through the combinational part and captured by storage element which is second source for SEU [3]. If a particle hits a control signal, such as the clock signal, it may generate a false control signal that can results in an unwanted data latch or timing violation [4]. The rate at which soft errors occur is referred to as soft error rate (SER).

Traditionally memories are protected by Error Correction Codes (ECC). Storage elements have also received more attention to make them more robust to soft errors [11]. However, recent studies indicate that logic is also going to be more vulnerable to soft error [2][5].

During the process of transient voltage propagation in logic gates, a SET may be masked by logical, electrical, or latching window -masking effects [5][20]. These masking mechanisms prevent some SETs from being latched and alleviate the soft error rate in digital systems. However, due to continuous scaling trends, increased frequency and wide spectrum of particle energy, the probability that a transient voltage reaches storage elements in capturing window and gets latched, is increasing and so does the soft error rate. Thus more circuit level hardening techniques are required.

The simplest form of hardening technique for logic as well as latches and flip-flops is to increase stored node charge by adding resistance or capacitance [8] which degrade circuit speed and increase power consumption.

Gate sizing to mitigate SET effect at logic level [15] as well as guard ring effect to reduce charge absorb efficiency[18], and negative feedback effect are studied [17]. The objectives of those studies are to design and size gates in the way that they attenuates transient voltages caused by particle strike.

While error-correcting codes and latch-hardening designs can be used to reduce the effect of SEU, complete protection against SET is much more difficult and involves either spatial or temporal redundancy. The spatial redundancy uses multiple copies of a given circuit with majority voting to determine

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correct outputs. One effective way to overcome SEU effects is to triplicate each latch of the system and use Triple Module Redundancy (TMR-latch). Although TMR-latches are highly reliable and widely used [6], this technique suffers from high area and energy consumption overhead.

The temporal redundancy technique is based on delayed sample of data, and is more suitable for conventional designs due to its lower power consumption. This technique can eliminate all SET pulses smaller than a certain threshold value. The major drawbacks of this method are its delay penalty, and the fact that it cannot guarantee fault-free operation for transients larger than a threshold point.

The dual interlock cell (DICE) is a soft error hardening circuit topology based on spatial redundancy and consists of two p-device and n-device loops. It has been introduced [9] and applied to a standard 6T memory cell [10] and used in pulsed latch [10][19]. The hardened feedback of DICE circuit has the potential to improve SEU robustness of the latch circuits without degrading its speed too much; however DICE comes with area and power penalty [19].

Redundant feedback loop is another soft error hardening method used in the basic latch design by replacing single feedback loop with dual feedback loop. According to [3], soft error of the internal nodes in feedback loop, i.e. B and C in Fig. 1, has the major contribution to the total SER. The particle strike may causes an unexpected voltage transient inside the feedback loop and alter the stored value in the latch. Our study and simulation result shows that node B is also much more sensitive than node C.

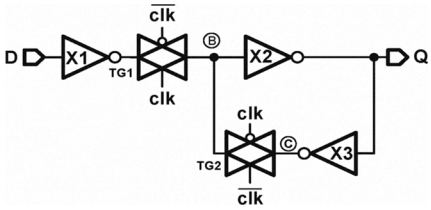

Fig. 1: Positive Level Sensitive Latch

The SIN-LC latch of **Fig. 2** (a) [3] is proposed to implement the dual feedback loop idea. It consists of redundant feedback loop and C-element. Besides to sizing issue, the SIN-LC suffers from contention current drawback that occurs when the latch is in the transparent mode. SIN-HR [3] of **Fig. 2** (b) is proposed to solve those problems, but the main problem still exists. The FERST [7] is another latch which is based on same idea and tries to solve contention problem, but it also comes up with large area, timing and power overhead.

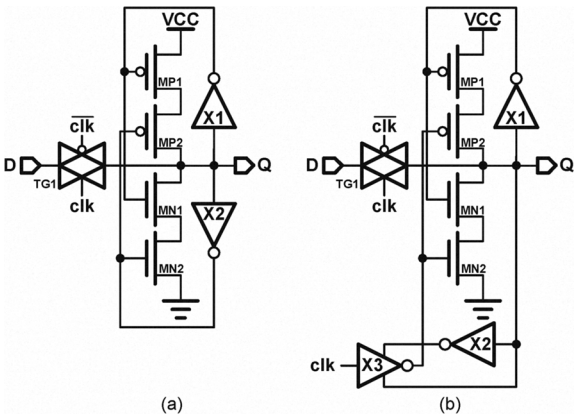

Fig. 2: Redundant Feedback Latch [3] (a) SIN-LC, (b) SIN-HR

Those aforementioned methods, as well as scan based SER resilient latch [16] and transient detection of RAZOR II flip-flop [14] are not able to tolerate soft errors due to capturing SET which results from particle hit on combinational logic. The transient filtering effect of Schmitt-trigger is also studied and a latch based on its property is proposed [11]. The transmission gate [13], negative feedback [17], and circuit layout effect on charge absorption coefficient and reduced soft error rate [18] are also reported separately. Skewed CMOS also has a built-in glitch filtering effect [21].

III. PROPOSED SOFT ERROR HARDENED LATCH

This section proposes a new soft error hardened edge triggered latch which is based on temporal redundancy, dual feedback loop and incorporates SET glitch filtering. The detailed schematic of proposed latch is shown in **Fig. 3**. It employs two C-elements and dual feedback loops to filter out particle strike effect. Data redundancy and glitch filtering effect of skewed CMOS is used to reduce SET coming from combinational logic. Input data filtering is done in two steps. At the first step, the data path is divided into two paths; each contains an inverter, X1 and X2. Those two inverters are skewed in different direction to shift voltage-transfer-curve one to the left and the other to the right side of mid-point. On the second path extra transmission gate is added to create temporal redundancy and more glitch filtering. At the second step, C-element is used to filter out more transients.

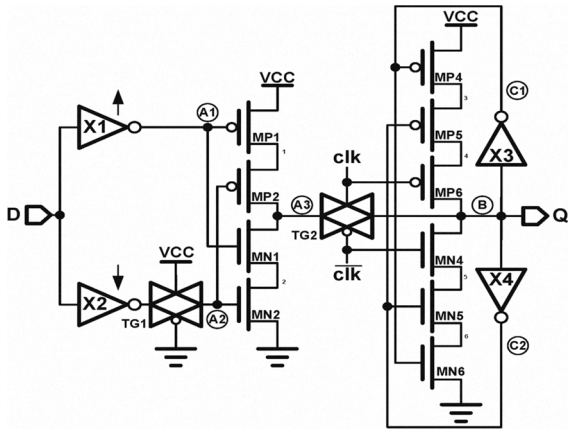

Fig. 3: The Soft Error Hardened Latch

The proposed circuit is an edge-triggered pulsed latch and operates in transparent and hold modes as follows. A general purpose pulse generator circuit is used to generate tiny pulses on each clock edges. With the small period of tiny pulses, MP6 and MN4 are turned-off, feedback loops are disconnected from output node and the latch is transparent. During transparent time, the skewed inverters produce the negative- and positive-glitch filtered version of input data. Those two data copies are applied to the C-element composed of MP1, MP2, MN1, and MN2. If both versions are the same, the output will change accordingly. In other words, the data will be latched on the condition that it is not a single transient.

After tiny pulse, the latch switches to the hold mode. In this mode data paths are blocked and feedback loops are closed. The sensitive nodes in the proposed circuit are C1 and C2. If a particle hit one of those nodes, it generates voltage spikes but dual feedback connection and the second C-element will remove its effect.

The required delay value to implement temporal redundancy should be longer than the duration of the possible longest SET in order to effectively filter it out. The timing diagram in **Fig. 4**(a) shows the positive setup time of an ordinary clocked storage element. Applying temporal redundancy increases this setup time (**Fig. 4**(b)) resulting in performance penalty. As a result, window of vulnerability (WOV) [3] to particle hit also increases. The proposed topology uses the resulted negative setup time of pulsed latches to mitigate setup time penalty. Applying the temporal redundancy to the pulsed latch (**Fig. 4**(c)) adds positive delay value to the negative setup time, thus the setup time of hardened pulsed latch in **Fig. 4**(d) is still smaller than ordinary latch. The simulation results of next section shows around 100ps improvement in the setup time.

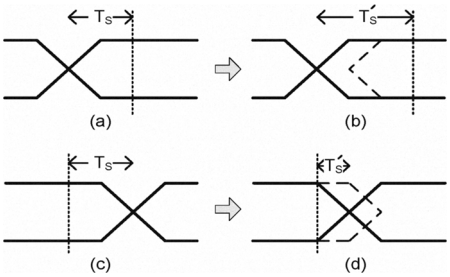

Fig. 4: Setup time (a) (b) ordinary clocking, (c) (d) Pulsed clocking

IV. Simulation Results

The proposed latch has been implemented using 90nm CMOS technology with 1.2V power supply voltage. In order to have realistic waveform and rise/fall times the simulation setup shown in **Fig. 5** is used for all cases [22].

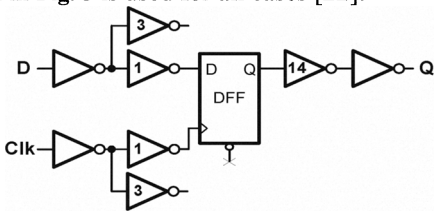

Fig. 5: Simulation Setup

The performance of the proposed latch has been verified in normal mode and particle strike mode. **Fig. 6** shows the circuit's normal operation timing result and shows its basic data to output delay (t_{DQ}) and setup time variation. This figure also gives the setup time and the t_{DQ} delay for ordinary latch of **Fig. 1**, and the proposed circuit in level sensitive and pulse clocked mode for comparison. The flat region on the data-to-output delay and negative setup time of the proposed latch reveals that if data arrive close to the clock edge or even 40ps after clock edge, the latch is still able to capture it correctly [12][22]. While same circuit in level sensitive mode and with almost same output delay comes up with large positive setup time. The extra negative setup time of the proposed circuit could be invested in the input data path by adding extra delay, to filter out more SETs.

The particle hit mode simulation is also divided in two modes. The first mode is SEU verification on internal nodes, which verifies robustness of the circuit against the particle hit on internal sensitive nodes. While the second mode verifies filtering effect and circuit robustness against the particle hit on combinational part and the resulted SET which reaches the latch on the sampling window.

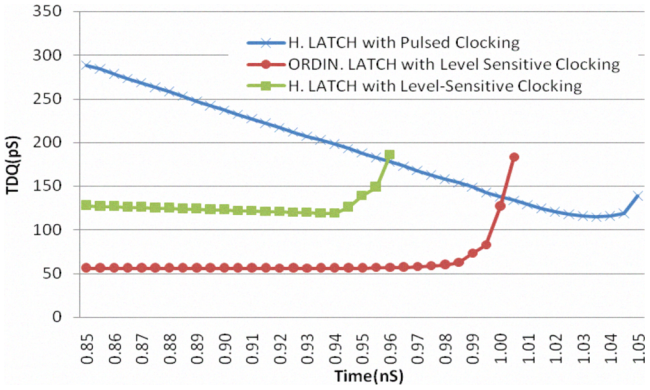

Fig. 6: Data to output delay and setup time variation of pulsed hardened latch, ordinary latch, and hardened latch with level-sensitive clocking.

Regardless of the particle type (alpha or neutron), it generates electron-hole pairs with high carrier concentration when it hits drain of the MOSFET and loses energy. The resulting charges can be rapidly collected by the electric field and create a large transient voltage at that node [1]. The whole process of charge deposit and distribution is complicated, but for sake of simplicity, it is modeled by a current source with exponential current level and varying time constants to emulate particles with different energy level [3][7].

The single particle hit on sensitive nodes is modeled by current injection at 1.5ns and 2.5ns, to the nodes C1 and C2 in **Fig. 3**, and nodes B and C in **Fig. 1**. The waveforms of **Fig. 7** shows the results and measurements on them indicates that the ordinary latch is unstable after 12.6fC and 19.8fC of charge injection into nodes B and C, respectively. While the dual feedback structure of proposed circuit is able to recover from almost any single particle hit and associated charge deposit.

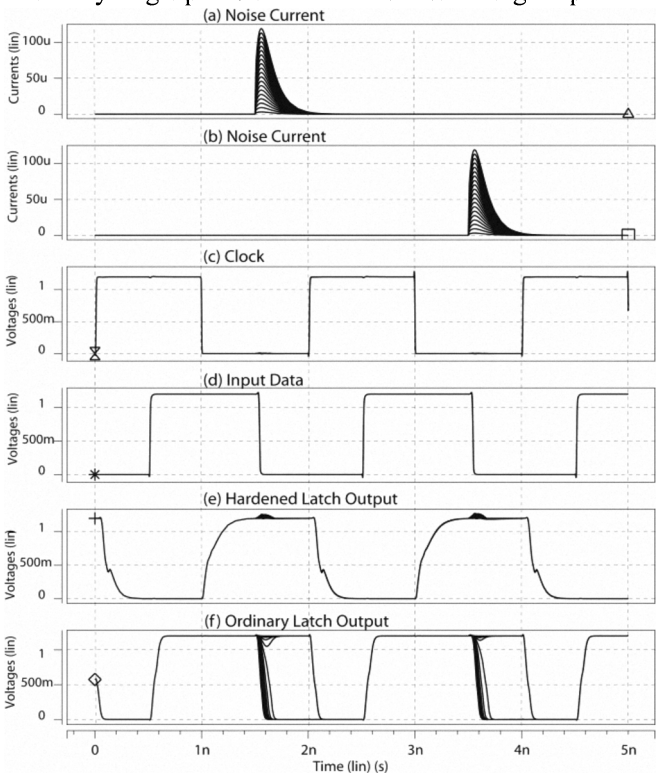

Fig. 7: Particle hit simulation result. (a), (b) Injected charge at 1.5ns, 3.5ns, (c) Clock, (d) Data, (e) Hardened latch output, and (f) Ordinary latch output.

The particle hit on combinational logic deposits charge which causes voltage glitch at gate's output. After passing levels of logics, those glitches convert to voltage pulses which may reaches to the latch "on-time" and gets captured. This phenomenon is modeled by voltage pulses on the data line with different width to represent various energy levels and circuit property. The arrival time of those pulses are tuned based on the setup and hold time of the proposed circuit. **Fig. 8** shows the results and indicated that the proposed latch is able to filter out SETs with up to 130ps pulse width.

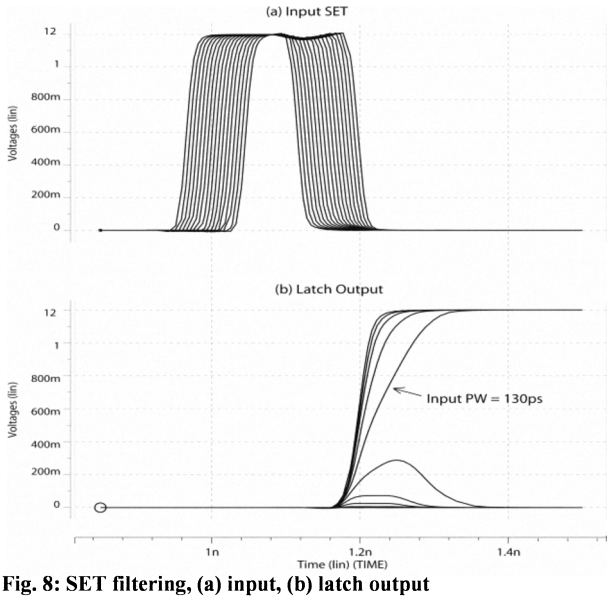

Fig. 8: SET filtering, (a) input, (b) latch output

The **Table I** also shows the setup time, data to output (t_{DQ}) delay and power consumption of the basic latch and the proposed circuit in level sensitive clocking and pulse-triggered mode for comparison.

Table I
Different latches' setup time, delay, power consumption and power-delay-product comparison

Latch Type	*Setup Time*	*Delay*	*Power*	*PDP*
Basic latch(Fig. 1)	50ps	56ps	5.83μW	0.32fJ
Fig. 3 in level sensitive	90ps	85ps	11.7μW	0.99fJ
Fig. 3 in pulsed mode	20ps	110ps	11.9μW	1.31fJ

V. CONCLUSION

In this work, an SER-Hardened latch has been proposed. The latch is based on noise filtering and redundancy. The circuit is able to tolerate particle strike on internal nodes as well as SET glitches occurring in combinational logic. The HSPICE simulation on 90nm CMOS technology is conducted to precisely evaluate the proposed circuit in normal mode and under particle strike mode. The circuit operates as an edge triggered flip-flop which is resilient to SET from combinational logic as well as SEU from internal nodes. In comparison with the other SER-hardened designs, proposed circuit has less power consumption and lower timing overhead which make it suitable for low-power reliable application.

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