A SINGLE-PHASE CLOCK HIGH-PERFORMANCE BICMOS LATCH

Borivoje Nikolic and Vojin Oklobdzija*

Department of Electrical and Computer Engineering, University of California, Davis, CA 95616, USA
*Integration, 1442A Walnut St. #412, Berkeley, CA 94709, USA

Abstract: A true single-phase clock BiCMOS latch intended for the use in high-performance deeply pipelined digital systems is proposed. It is based on quasi-complementary BiCMOS circuit, and uses single-phase clock. The speed and power performance of this latch are superior to previously published results, which has been shown by simulation in 0.8μm technology.

1. INTRODUCTION

BiCMOS digital circuits are often used in digital systems where high performance is of great importance. The overall speed of those systems is enhanced by deep pipelining and the use of relatively small number of logic stages. Fig. 1 shows the diagram of single-phase clocked pipelined system, consisting of two logic blocks separated by N and P type latches. N type latches are transparent when $\phi = 1$, and opaque when $\phi = 0$, while P type latches are transparent when $\phi = 0$, and opaque when $\phi = 1$ [1]. Since the pipeline design is based on latches [2, 3], they play the key role in overall system performance. If the latch is followed by a small number of logic stages, a high fan-out is often created, placing a demand for high driving capabilities of the latch. In this work, we propose a latch implemented in BiCMOS technology which improves the circuit performance in terms of speed and power. It is based on quasi-complementary (QC) BiCMOS inverter [4], and is suitable for low supply voltage operation. The latch is designed for use in true single phase clocked (TSPC) systems, and as opposed to the master-slave latch proposed in [5], which uses both phases of the clock. Its other advantage is the possibility of incorporating logic function into the latch [3]. It is compared to previously published results [3, 7], in terms of speed, power and dependence on supply voltage.

2. A NEW BICMOS LATCH

Performance of the conventional BiCMOS circuits degrades at low supply voltages. The QC-BiCMOS inverter overcomes that problem, without using a PNP transistor to restore the full swing. In this circuit, the PNP transistor is substituted by PMOS-NPN Darlington configuration, resulting in smaller dependence in pull-down operation of the circuit [3]. It has separate pull-up and pull down networks, thus the latch can be integrated in their CMOS parts.

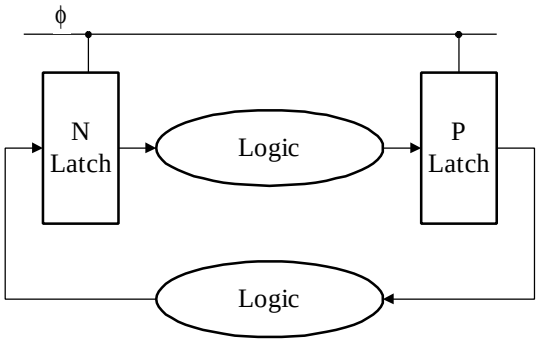

Figure 1: Single-phase pipeline

TSPC technique is commonly used in high performance digital systems due to its simplicity and fast operation [3]. Four basic stages exist in TSPC, precharged N and P, and nonprecharged N and P, as shown on Fig. 2.

By combining these stages latches and flipflops can be formed. For example, N type latch consists of two nonprecharged N stages. However, driving capability of the CMOS implementation of the TSPC latch is limited and the latch itself is susceptible to noise. Our objective was to improve its driving capability and eliminate the floating nodes, which makes the latch more robust.

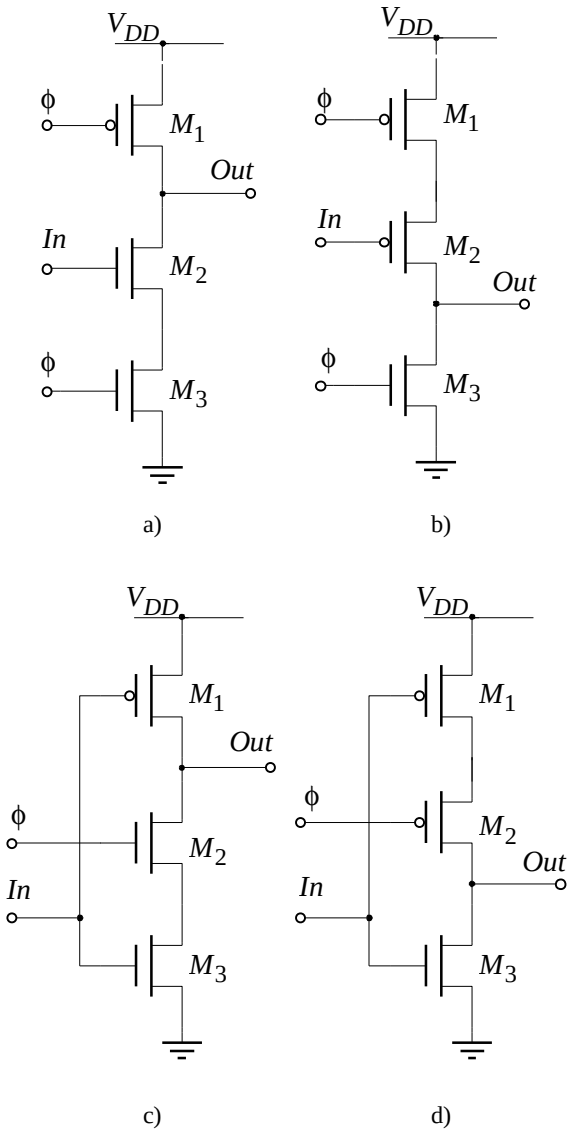

Figure 2: Basic CMOS TSPC stages: a) precharged N, b) precharged P, c) nonprecharged N, d) nonprecharged P.

A. Latch operation

The new BiCMOS implementation of the TSPC N section is shown on Fig. 3. Transistors M1 - M3 and M4 - M6 form the N-section of the CMOS TSPC N stage in pull-up and pull-down networks. They are transparent when $\phi = 1$ and perform latching when $\phi = 0$. The advantage of this design is that logic function blocks can be included in the latch, by placing them instead of M1, M4 and M3, M6 [3]. Full latches and flip flops can be designed by combination of CMOS and BiCMOS stages, in the way it is described in [3]. The BiCMOS part is based on original QC-BiCMOS, with additional improvement by replacing resistors by transistors M7 and M9, which is done in similar way as in [6]. These transistors are biased in the way to be off during the corresponding pull-up or pull-down operation to allow

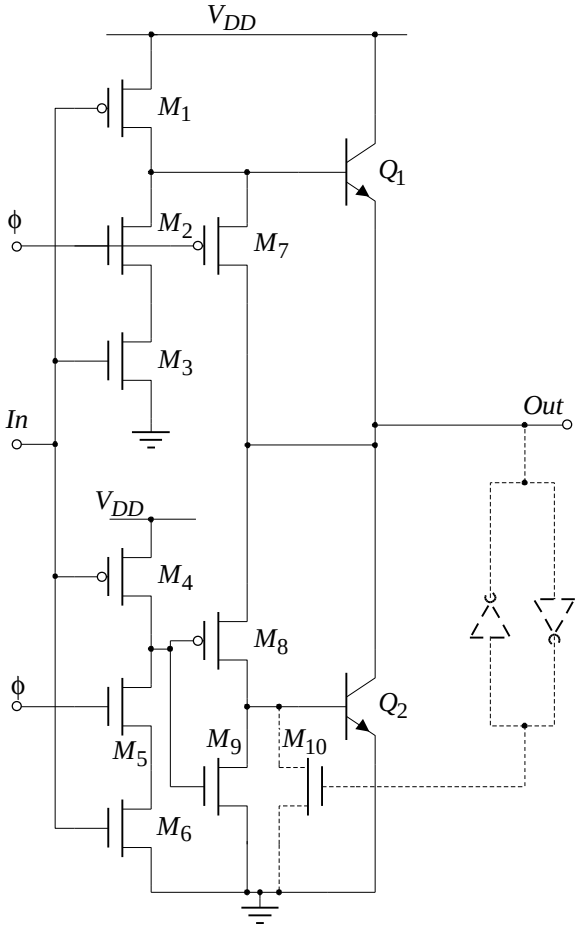

Figure 3: N type TSPC section.

steep transition until the output reaches the supply rail, by keeping the charge stored in the base of bipolar transistors. Addition of transistor M10 together with cross-coupled inverters at the output improves rise and fall times [4, 6], but increases the propagation delays. These inverters also allow the latch to be used as fully static, and not only as a TSPC pipeline stage. In that case the logic level at the end of the clock phase is latched on the output node.

The P type section, which is transparent when $\phi = 0$, is designed in similar way, by replacing the CMOS TSPC N section with P section, as shown on Fig. 4.

Precharged (dynamic) BiCMOS circuits of N and P type are analyzed in [6].

B. Circuit Performance

For the performance evaluation the N type latch consisting of the CMOS N stage and BiCMOS N stage is designed. The circuits are simulated using Hspice in 0.8μm BiCMOS technology. All the transistors had minimal gate length of 0.8μ, NMOS transistors were 10μm wide and PMOS transistors were 20μm wide. The characteristic output waveforms are given on Fig. 5.

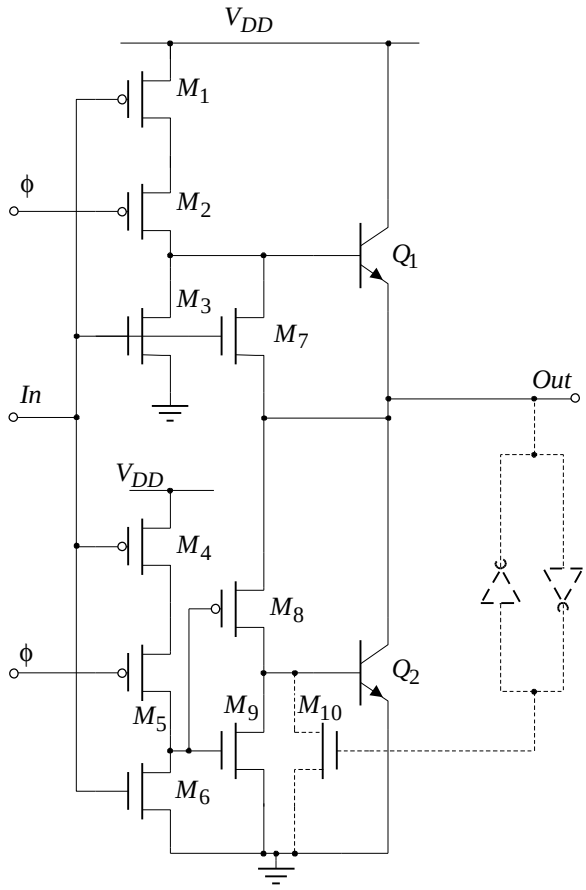

Figure 4: P type section

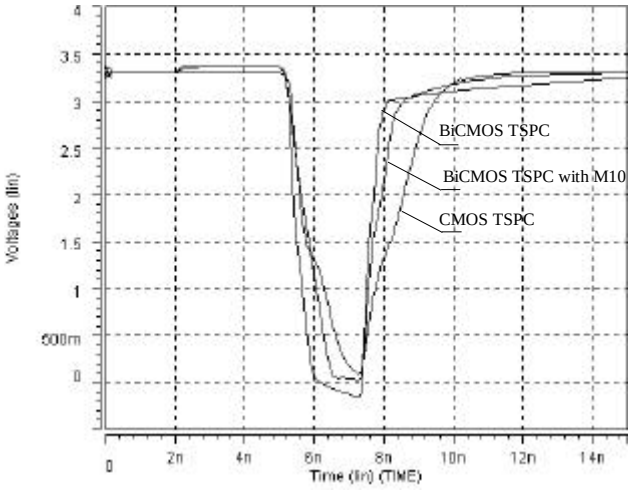

Figure 5: Output waveforms of a) new BiCMOS TSPC stgae, b) new BiCMOS TSPC stage with M10, c) CMOS TSPC stage, loaded with 8 CMOS inverters (400fF) at 100MHz

The loads used in all simulations that determined the driving capability were the CMOS inverters with W_p/W_n = 20µ/10µ, which had equivalent input capacitance of approximately 50fF.

The driving performance is compared to TSPC latch implemented in CMOS [3], and with the latch proposed in [7], with the same transistor sizes. The new latch is always faster and dissipates less power than latch published in [7], and is faster than CMOS for fan-outs bigger than 2. The Fig. 6 shows the dependence of the average delay from data and clock to the output for these circuits.

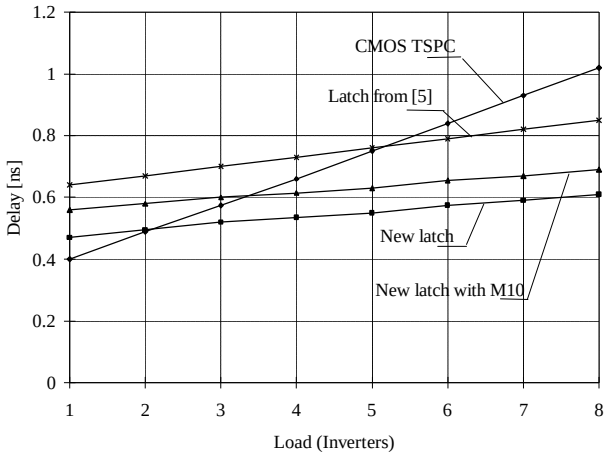

Figure 6: Delays from data/clock to output vs. load for a) new N type latch, b) new latch with M10, c) CMOS TSPC N latch, d) latch from [5].

The proposed circuits are is suitable for the use with as low as 1.5V supply voltage. The BiCMOS latch delay is smaller than its CMOS implementation at supply voltages from 1.5V to 5V, as shown on Fig. 7. The comparison is done with the load of four inverters.

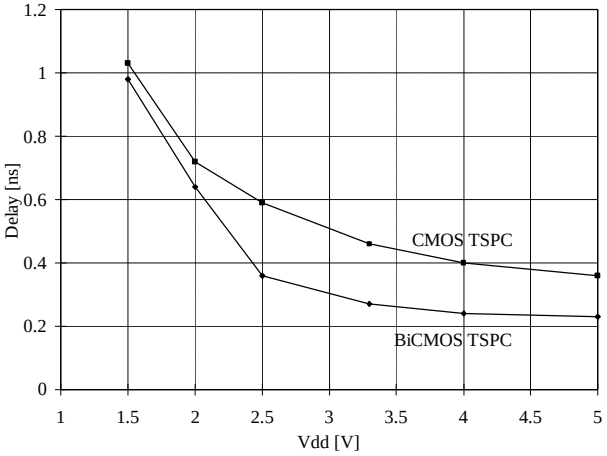

Figure 7: Comparison of BiCMOS and CMOS TSPC N stage delays having fanout of 4 vs. supply voltage.

This proposed BiCMOS latch has significant power savings compared to CMOS implementation for the fan-outs larger than 3. Fig. 8 shows the power consumption comparison between BiCMOS and CMOS

stage in respect to the fan-out where the size of the CMOS stage was adjusted to match the delays. The reason for this savings in power is that the bipolar transistors in the QC stage conduct current for a short amount of time, quickly charging/discharging the output node [4]. The CMOS stage needs significantly larger sizes of the transistors to achieve the same delay with bigger loads, which also increases the loading capacitance at the output and results in longer rise and fall times.

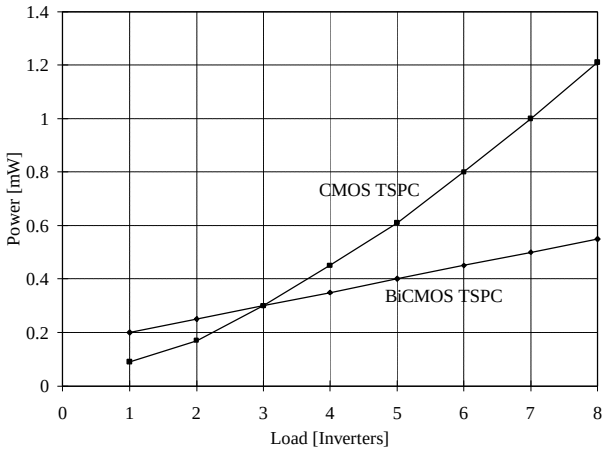

Figure 7: Comparison of power consumption for CMOS and BiCMOS implementations of the latch with respect to the load.

3. CONCLUSION

The advantage of the true single-phase clocking design is significantly improved when the TSPC latch is implemented in BiCMOS. This paper has shown the design and analyzed the performance of the new latch, which can be utilized in high performance systems. It has smaller average delay than previously published circuits, with smaller power dissipation. Generally it has advantage in speed and power to its CMOS counterpart in driving fanouts larger than 3. This improves the performance of deeply pipelined systems that inherently produce larger fan-outs, thus requiring larger driving capabilities.

REFERENCES

[1] D. W. Dobberpuhl, *et al*, "A 200MHz 64-b Dual-Issue CMOS Microprocessor," *IEEE JSSC*, vol. 27, no. 11, 1992, pp. 1555-1567.

[2] N.F. Goncavles, H.J. De Man, "NORA: A Racefree Dynamic CMOS Technique for Pipelined Logic Structures," *IEEE JSSC*, vol. SC-18, 1983, pp. 261-266.

[3] Y. Ji-Ren, I. Karlsson, C. Svensson, "A True Single-Phase-Clock Dynamic CMOS Circuit Technique," *IEEE JSSC*, vol. SC-22, 1987, pp. 261-266.

[4] K. Yano, *et al*., , "Quasi-Complementary BiCMOS for Sub-3V Digital Circuits," *IEEE JSSC*, vol. 26, 1991, pp. 1708-1719.

[5] K. Yano, *et al*. "3.3V BiCMOS Circuit Techniques for 250MHz RISC Arithmetic Modules," *IEEE JSSC*, vol. 27, no. 3, 1992, pp. 373-381.

[6] S.S. Lee, M. Ismail, "1.5V Full-Swing BiCMOS Dynamic Logic Circuits," IEEE Trans. on CAS - I: Fundamental Theory and Applications, vol. 43, 1996, pp. 760-768.

[7] J.B. Kuo, J.H. Lou, K.W. Su, "A High-Speed 1.5V Clocked BiCMOS Latch for BiCMOS Dynamic Pipelined Digital Logic VLSI Systems," *Proceedings of Eighth Annual IEEE International ASIC Conference and Exhibit*, 1995, pp. 315-317.