

Clocked CMOS Adiabatic Logic with Integrated Single-Phase Power-Clock Supply: Experimental Results

Dragan Maksimović¹, Vojin G. Oklobdžija², Borivoje Nikolić², K. Wayne Current²

¹Department of Electrical and Computer Engineering, University of Colorado, Boulder, CO 80309-0425

²Department of Electrical and Computer Engineering, University of California, Davis, CA 95616

ABSTRACT

In this paper we describe the design and experimental evaluation of a clocked CMOS adiabatic logic (CAL). CAL is a dual-rail logic that operates from a single-phase AC power-clock supply in the 'adiabatic' mode, or from a DC power supply in the 'non-adiabatic' mode. In the adiabatic mode, the power-clock supply waveform is generated using an on-chip switching transistor and a small external inductor between the chip and a low-voltage DC supply. Circuit operation and performance are evaluated using a chain of inverters realized in 1.2 μ m technology. Experimental results show energy savings in the adiabatic mode versus the non-adiabatic mode at clock frequencies up to about 40MHz.

1 INTRODUCTION

The potential for energy savings using energy-recovery (or 'adiabatic') circuits has been examined using various circuit implementations [1-11]. Weaknesses of the previously proposed approaches include the need for multi-phase AC power-clock supplies for proper interfacing between stages, and correspondingly high complexity of both the logic and the required power-clock generator [1-9].

This paper describes results of experimental evaluation of the clocked adiabatic logic (CAL) [10,11] operated from a single-phase power-clock generator integrated with logic [11]. The measurements are focused on verification of operation of the logic over frequency and supply voltage ranges and a comparison of CAL energy consumption to the case when the logic is operated from a DC power supply.

Permission to make digital/hard copy of all or part of this work for personal or classroom use is granted without fee provided that copies are not made or distributed for profit or commercial advantage, the copyright notice, the title of the publication and its date appear, and notice is given that copying is by permission of ACM, Inc. To copy otherwise, to republish, to post on servers or to redistribute to lists, requires prior specific permission and/or a fee.
©1997 ACM 0-89791-903-3/97/08...\$3.50

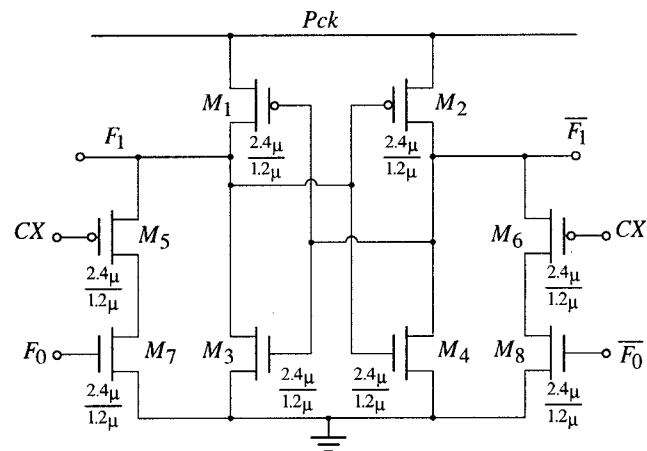


Figure 1: CAL inverter.

CAL circuit configuration and operation are reviewed in Section 2. Implementation issues and the test chip are discussed in Section 3. Measurement results are presented in Section 4. Section 5 concludes the paper.

2 CIRCUIT OPERATION

The basic CAL gate, the inverter, is shown in Fig. 1. Cross-coupled CMOS inverters, transistors M_1 - M_4 , provide the memory function. In general, the devices M_7 and M_8 can be replaced with NMOS logic trees to perform switching involved in the evaluation of an arbitrary binary function. As an example, implementation of a 2:1 MUX stage is shown in Fig. 2. The CAL topology is similar to the logic proposed by Denker [6]. Our innovation is the inclusion of path control switches, devices M_5 and M_6 , added in series with the logic trees. This modification allows operation of the circuit with a single-phase power-clock supply, Pck , as opposed to the four-phase power clock required by the logic proposed in [6].

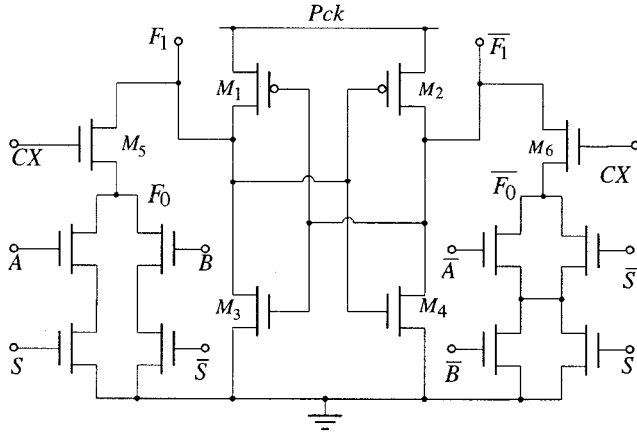


Figure 2: 2:1 MUX implemented with CAL.

Idealized CAL timing waveforms for the inverter are shown in Fig. 3. The power clock Pck is shown as a trapezoidal waveform. Logic evaluation is enabled by the auxiliary clock CX . For $F_0 = 0$, M_7 is off, M_8 is on, the complementary output $\overline{F_1}$ goes to 0, and the true output F_1 follows the power-clock waveform. In the next clock period, the auxiliary clock $CX = 0$ disables the logic evaluation and the outputs repeat the result stored during the evaluation in the previous clock period. As a result, the CAL logic states are represented by presence or absence of a pair of pulses. When controlling a chain of logic stages, the same power clock Pck supplies all CAL stages. The logic evaluation is enabled in alternate logic stages by the auxiliary clock CX and its complement \overline{CX} . To reduce power consumption in the auxiliary clock distribution, the swing of the auxiliary clocks can be reduced without affecting the signal levels in the logic. It is interesting to note that CAL can also be operated as a conventional clocked logic with a DC power supply connected to Pck .

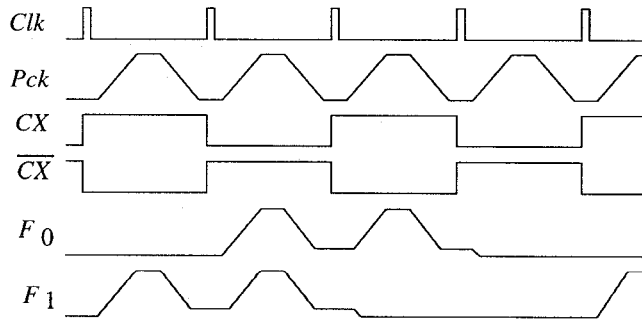


Figure 3: Idealized CAL timing waveforms.

3 IMPLEMENTATION

Fig. 4 is a block diagram of the experimental CAL chip built as a chain of $n = 736$ dual-rail inverters in $1.2\mu\text{m}$ CMOS technology. Fig. 5 shows the test chip die photo.

The device sizes in the CAL logic stages are indicated in Fig. 1 and Fig. 4. For testing purposes, twelve of the inverters have both outputs connected to the output pins, via conventional output buffers that serve as voltage comparators. The conventional output buffers and the circuits used to generate the auxiliary clocks are supplied from a separate DC supply V_{DD} . The inductor L and the low-voltage DC source V_B are used for energy-recovery (adiabatic) operation of the CAL chip. The AC power-clock waveform Pck is generated using a single NMOS device Q in parallel with the CAL logic. The device Q is turned on during a small fraction of the clock period at the point when Pck is approximately zero. During this time, energy is added to sustain oscillation in the resonant circuit formed by the external inductance L and the equivalent logic capacitance C_{eq} . When Q is clocked close to the resonant frequency, Pck swings between 0 and a peak value approximately equal to $2 \cdot V_B$ [11]. The switching transistor Q takes a small fraction of the total chip area, as shown in Fig. 5, where Q is the area immediately to the left from the CAL label.

Given a desired power-clock frequency f , the required inductance L can be found from

$$f = \frac{1}{2\pi\sqrt{LC_{eq}}},$$

where $C_{eq} = 101\text{pF}$ is the measured equivalent chip capacitance at the Pck node. The equivalent chip capacitance was measured by connecting a resistor R between V_B and Pck and by measuring the time constant RC_{eq} of the charge-up transient after the device Q is turned off. The logic can also be operated from a DC supply connected directly to Pck , while the power-clock device Q is disabled. This non-adiabatic mode of operation is used to evaluate how much energy can be recovered by the power clock.

4 EXPERIMENTAL RESULTS

Operation of the circuit is illustrated by the waveforms shown in Fig. 6 for an input sequence of 1100 and two power-clock frequencies. The pair of quasi-sinusoidal pulses that corresponds to the logic high output is observed as a pair of rectangular pulses through the conventional, DC-supplied output buffers. The maximum operating frequency of the circuit in this test configuration was 50MHz, due to signal source limitation. Higher operating frequencies are predicted by simulation [10].

Energy consumption of the CAL chip (excluding the consumption of the output buffers) was measured as a function of frequency for three cases: (1) for adiabatic operation when 3V peak-to-peak sinusoidal Pck was supplied from an external function generator and the on-chip power-clock device Q was disabled; (2) for adiabatic operation with quasi-sinusoidal Pck generated using $V_B = 1.5\text{V}$ and an external L , and by clocking Q as shown in Fig.3; and (3) for non-adiabatic operation with the minimum DC supply voltage $V_B = 2.5\text{V}$ for which the DC-

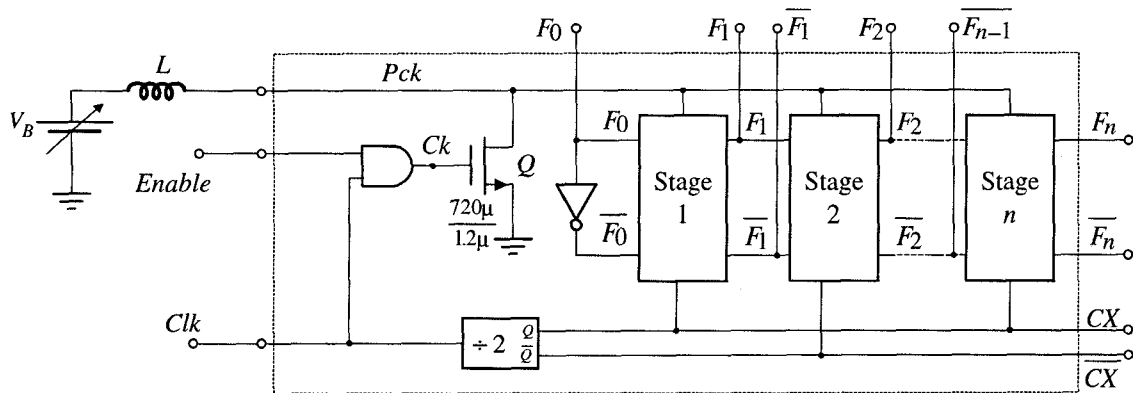


Figure 4: A chain of CAL logic gates with on-chip power-clock generation. For adiabatic operation, $Enable = 1$, and inductor L is connected between Pck and the DC supply V_B ; for non-adiabatic operation, $Enable = 0$ and $Pck = V_B$.

supplied logic was found to function properly. In all three cases, the activity factor (defined as the normalized number of input transitions) is equal to 1. The results are shown in Figs. 7 and 8. The non-adiabatic energy consumption is approximately constant at about 0.58pJ per inverter per cycle. The theoretical non-adiabatic energy consumption, based on the measured $C_{eq} = 101\text{pF}$ is 0.61pJ per inverter per cycle. The small difference comes from the fact that C_{eq} includes capacitance of the Pck distribution, which is not switched during non-adiabatic operation. These results show that the energy consumption of the CAL operated from the DC supply is indeed equal to CV^2 losses. Therefore, the results of Fig. 7 show how much of the CV^2 can be recovered through the power clock during adiabatic operation of the chip with external or internal power clock. Energy savings are very large at low operating frequencies and diminish as the frequency approaches $f = 30\text{MHz}$. The results with the externally supplied power-clock waveform are significantly better than the results with the internally generated Pck . We believe that significantly better performance of the internal power-clock generator can be obtained by increasing the size and reducing the on-resistance of the switching transistor Q .

By changing the activity factor at a constant power-clock frequency it was found that the CAL power consumption at the activity factor equal to 0 is approximately one half of the power consumption at the activity factor equal to 1, as shown in Fig. 8. This confirms that at low activity factors non-adiabatic operation from a DC supply can be significantly more efficient.

The CAL ability to operate from either a single-phase AC power-clock supply or from a DC supply opens interesting possibilities to combine adiabatic and non-adiabatic modes of operation to achieve energy-efficient

operation for a very wide range of throughput rates and activity factors.

The energy consumption measurements shown in Figs. 7 and 8 included only the part of the circuit operated from the supply V_B : the logic and the switching transistor Q . The measured energy consumption per cycle of the circuits supplied from the constant DC voltage $V_{DD} = 3\text{V}$ (auxiliary clocks and the driver for the switching transistor Q) is about 30pJ, or about 8% of the total non-adiabatic energy consumption.

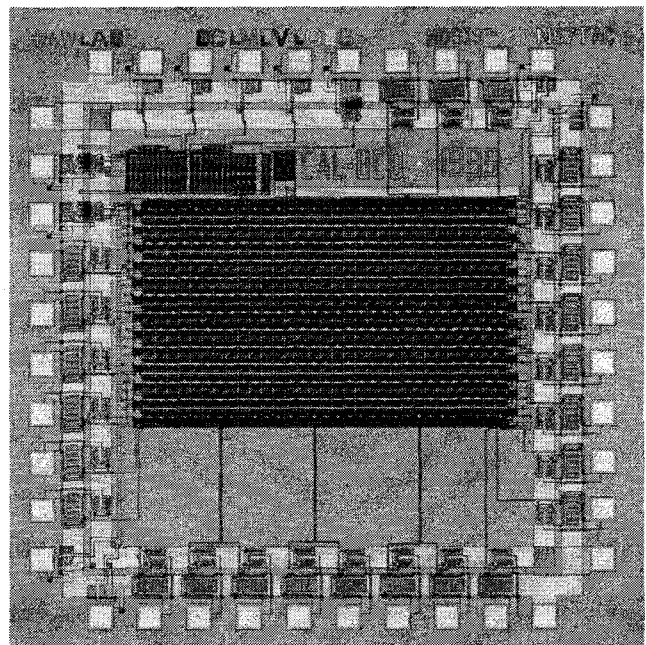
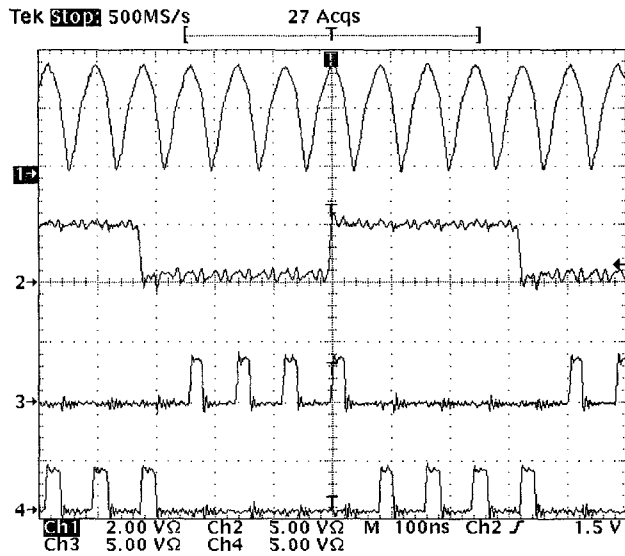
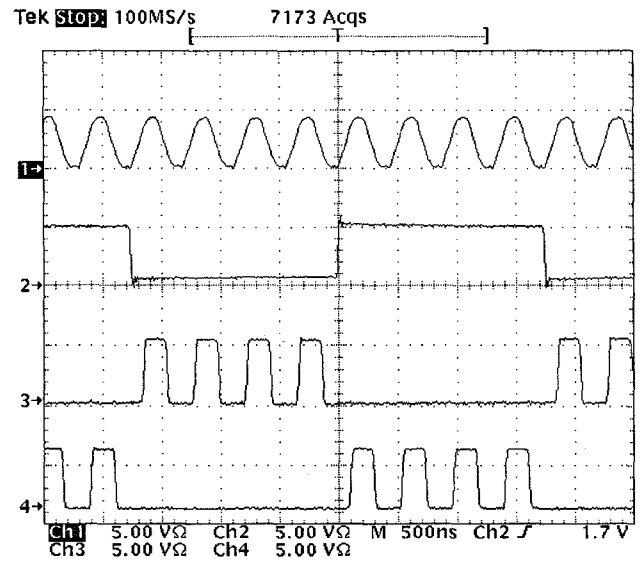


Figure 5: Test chip die photo.



(a)



(b)

Figure 6: Measured CAL waveforms: Ch1: power clock Pck , Ch2: logic input F_0 , Ch3: buffered logic output F_1 , Ch4: buffered complementary logic output $\overline{F_1}$ for (a) $f = 12.5\text{MHz}$, the logic is supplied from $V_B = 1.8\text{V}$, while the DC supply for the conventional output buffers is $V_{DD} = 4\text{V}$ and (b) $f = 2.36\text{MHz}$, the logic is supplied from $V_B = 1.5\text{V}$, the DC supply for the output buffers is $V_{DD} = 5\text{V}$.

5 CONCLUSION

The proposed clocked adiabatic logic (CAL) operates from a single-phase power-clock supply. The test chip, a chain of inverters, is implemented in a $1.2\mu\text{m}$ CMOS technology. Operation of the logic and its energy consumption are measured for adiabatic operation using an external power-clock generator or using a simple on-chip power-clock generator. These results are compared to the energy consumption measured in non-adiabatic operation when the

chip is supplied from a DC voltage source. Experimental results show significant energy savings at relatively low clock rates. The CAL ability to operate from either AC power-clock supply or from a conventional DC supply opens further possibilities for energy-efficient operation in a very wide range of throughput rates by combining adiabatic and non-adiabatic modes of operation.

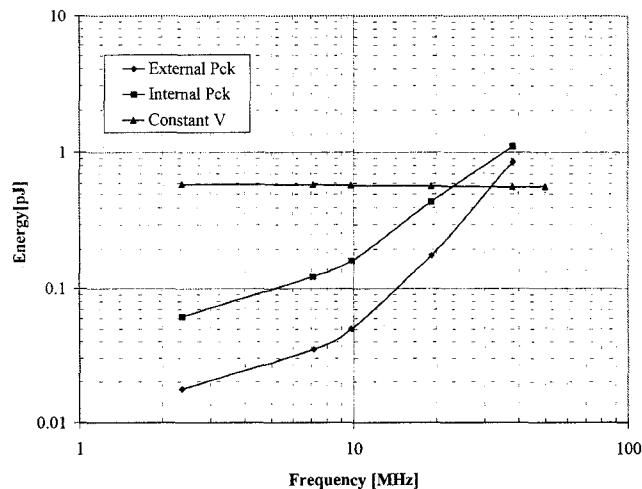


Figure 7: Energy/inverter per cycle vs. frequency.

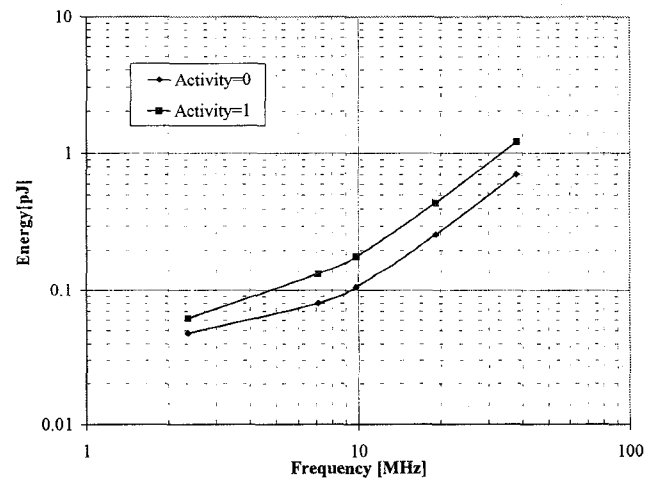


Figure 8: Energy/inverter vs. frequency for different activity factors.

ACKNOWLEDGMENTS

The authors would like to thank Fengchen Lin and Olivier Greneche for their help in layout and testing of the CAL chip.

REFERENCES

- [1] A.G. Dickinson, J.S. Denker, "Adiabatic Dynamic Logic," *IEEE Journal of Solid-State Circuits*, vol. 30, no. 3, pp. 311-315, March 1995.
- [2] T. Gabara, "Pulsed Low Power CMOS," *International Journal of High Speed Electronics and Systems*, vol. 5, no. 2, pp. 159-177, June 1994.
- [3] J.G. Koller, W.C. Athas, "Adiabatic Switching, Low Energy Computing and Physics of Storing and Reading of Information," *Proceedings PhysComp '92*, Dallas, Texas, Oct. 2-4, 1992.
- [4] W.C. Athas, L.J. Svensson, J.G. Koller, N. Tzartzanis, E. Y.-C. Chou, "Low-Power Digital Systems Based on Adiabatic-Switching Principles," *IEEE Transactions on VLSI Systems*, vol. 2, no. 4, December 1994.
- [5] S.G. Younis, T. Knight, "Practical Implementation of Charge Recovering Asymptotically Zero Power CMOS," *Proceedings of 1993 Symposium on Integrated Systems*, pp. 234-250, MIT Press, 1993.
- [6] J.S. Denker, "A Review of Adiabatic Computing," *Proceedings of the 1994 Symposium on Low Power Electronics*, San Diego, October 1994.
- [7] A. Kramer, J.S. Denker, S.C. Avery, A.G. Dickinson, T.R. Wik, "Adiabatic Computing with the 2N-2N2D Logic Family," *IEEE Symposium on VLSI Circuits, Digest of Technical Papers*, pp. 25-26, 1994.
- [8] R.T. Hinman, M.F. Schlecht, "Recovered Energy Logic - a Highly Efficient Alternative to Today's Logic Circuits," *IEEE Power Electronics Specialists Conference*, 1993.
- [9] Y. Moon, D-K. Jeong, "An Efficient Charge Recovery Logic Circuit", *IEEE Journal of Solid-State Circuits*, vol. 31, no. 4, pp. 514-522, April 1996.
- [10] D. Maksimović, V.G. Oklobdžija, "Clocked CMOS Adiabatic Logic with Single AC Power Supply," 21st *European Solid State Circuits Conference, ESSCIRC'95*, Lille, France, September 1995.
- [11] D. Maksimović, V.G. Oklobdžija, "Integrated Power Clock Generators for Low-Energy Logic," 26th *Annual IEEE Power Electronics Specialists Conference*, Atlanta, June 1995.