Low-Energy Logic Circuit Techniques for Multiple Valued Logic

K. W. Current*, V. G. Oklobdzija*, and D. Maksimovic+

*Electrical and Computer Engineering Department
University of California
Davis, CA 95616

+Electrical and Computer Engineering Department
University of Colorado
Boulder, C0 80309

Abstract

Multiple valued logic (MVL) has been proposed as a means for reducing the power, improving the speed, and increasing the packing density of VLSI circuits. These performance improvements are achieved by designers who identify signal processing functions that can benefit from the design tradeoffs possible with MVL. Since advocates of MVL are accustomed to incorporating the possible tradeoffs of MVL techniques into specific VLSI design applications, these MVL designers may be able to take advantage of new energy saving circuit design techniques that may have tradeoffs that complement those of MVL.

Low-energy (adiabatic) logic circuits have been proposed to reduce energy consumption of VLSI logic functions. Instead of the conventional dc power supply, these logic circuits use "ac" power supplies (power clocks) that allow energy recovery and also serve as timing clocks for the logic. It is possible to integrate all power switches and control circuitry on the chip with the low-energy logic. This results in better system efficiency and simpler power distribution. In this paper, concepts of adiabatic circuit design and the use of a high-frequency resonant power clock generator for adiabatic circuits will be summarized and then their possible application to low-energy, adiabatic Multiple Valued Logic is discussed.

Introduction

High-speed VLSI chip design challenges increasingly involve the reduction of energy consumption. This is motivated in part by increasing difficulties in removal of chip heat, increasing need for energy-limited, battery-operated applications, and an overall concern for limiting energy usage. Various low-energy logic families have been proposed [1-7] to address these concerns. Instead of the conventional dc power supply, low-energy, or recovered-energy or adiabatic, logic families require ac supply voltages that allow energy recovery and also serve as timing clocks for the logic. A "power clock generator" is the high-frequency resonant power converter used to supply energy to the logic. Thus, an efficient power clock generator is needed to help practically realize the potential advantages of adiabatic logic. We are interested in applications of low-energy logic in low-power, battery-operated systems where energy efficiency is one of the main performance parameters, and where a battery is available.

The usefulness of an ac power supply can be understood by examining the energy dissipated in the charging/discharging of a load capacitance through a series resistance. If the excitation voltage is a single step of amplitude V_0, the energy dissipation is $0.5CV_0^2$. If the load capacitor is charged with 2 step inputs of amplitude $0.5V_0$, the energy dissipated is $0.25CV_0^2$. If the load capacitor is charged with n step inputs of amplitude $(1/n)V_0$, the energy dissipated is $(1/2n)CV_0^2$. Charging the load capacitor with a ramp of voltage will dissipate energy of approximately $(\tau/T)CV_0^2$, where τ=RC and T is the charging time which is much greater than τ. We see that the longer the time used to charge the capacitor, the less energy dissipated. Another design tradeoff that may be exploited has been introduced. Thus, as a simple matter of energy dissipation, a triangular charging/discharging waveform applied to the load capacitor will dissipate less energy than a square wave applied to the load capacitor. If the premise is accepted that a triangular (or sinusoidal) oscillating power supply voltage could be useful in reducing the energy dissipated in logic circuits, then we could make the oscillator an LC resonant circuit that can re-capture during the capacitor discharge interval some of the energy that was supplied during the capacitor charge interval.

In the next section, example binary adiabatic circuits and a resonant power clock are reviewed. Then we discuss the application of principles of adiabatic circuits to MVL.

Binary Adiabatic Logic Circuit Examples

Common to all low-energy (adiabatic) logic families is the periodic exchange of energy between the power clock generator and the logic. Logic evaluation follows one of several possible approaches including the use of *memory* schemes [6]. Although logic with energy loss that asymptotically approaches zero is feasible [2], memory schemes with partial energy recovery [3-7] are preferred because of their much simpler circuitry and more area-efficient implementation. In memory schemes, each logic stage also performs a memory function so that logic outputs can remain valid even without valid logic inputs. Assuming the use of standard CMOS transistors, an energy loss in the order of $C|V_t|^2$, where $|V_t|$ is the device threshold voltage, accompanies each logic transition when the memory in the

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adiabatic circuit is erased [1]. This is about an order of magnitude lower loss than the CV_{DD}^2 loss in conventional standard CMOS logic circuits, at a voltage level of V_{DD} = 3V and $|V_t|$ < 1V. Memory schemes offer inherent pipelining, but can require multi-phase power clocks.

Binary Adiabatic Logic with Multiple Phase Power Clocks. A representative binary CMOS adiabatic logic inverter example [6] is shown in Figure 1. This inverter has complementary logical inputs, F0 and $\overline{F0}$, and outputs F1 and $\overline{F1}$. The stage consists of a flip-flop (M1-M4) and devices that implement the logic function. M5 and M6 implement an inverter in this figure. Arbitrary multi-input logic functions can be realized by replacing devices M5 and M6 with appropriate NMOS logic trees. The stage is supplied by the power clock PCK, shown in Figure 1 as an idealized trapezoidal waveform. During the *evaluate* interval A, inputs F0 and $\overline{F0}$ must retain their valid logic levels. In the example in Figure 1, as PCK ramps up, the output F1 stays at zero, while energy is delivered from the power clock to the node capacitance at the complementary $\overline{F1}$ output. During the *hold* interval B, the outputs F1 and $\overline{F1}$ remain valid, while the inputs may change toward zero. In the *precharge* interval C, the output $\overline{F1}$ is discharged from VDD toward zero, partially returning energy from the node capacitance to the power clock generator. M2 in the discharge path turns off when PCK falls below the device threshold voltage $|V_t|$. Therefore, a part of the energy remains stored on the node capacitance at the $\overline{F1}$ output. In the *idle* interval D, the inputs may assume new valid values. A change in the logic input causes a loss of the residual energy at the $\overline{F1}$ output, through M6. Just as in resonant power converters, any additional energy losses are due to non-zero forward voltage drops on elements in the conducting path. These losses can be reduced arbitrarily by reducing the current magnitudes: for example, by decreasing the clock frequency, or by reducing the device on-resistances.

In a cascade connection of the logic stages, it is necessary to ensure that the *hold* interval of one stage coincides with the *evaluate* interval of the next stage. Therefore, four phase-shifted power clock waveforms are needed for proper stage-to-stage interface. The system timing for a chain of logic stages uses four power clock waveforms PCK, PCK1, $\overline{PCK}$ and $\overline{PCK1}$ that are phase-shifted by one-fourth of the clock period.

Several other adiabatic low-energy logic families have been proposed with similar power clock requirements [4-7]. The problem of efficiently generating and distributing the multiple phase power clocks clearly becomes a limiting factor for these low-energy logic schemes.

Binary Adiabatic Logic with a Single Power Clock. An adiabatic inverter (or other logic function) that uses a single power clock [8], can be realized as shown in Figure 2. Auxiliary timing control clock signal CX controls transistors M7 and M8 that are in series with the logic trees represented by M5 and M6 in Figures 1 and 2. The CX-enabled devices M7 and M8 allow operation with a single power clock PCK. The idealized timing waveforms are shown in Figure 2. In the clock period A, the auxiliary clock CX enables the logic evaluation. For F0 = 0, M8 and M6 are on causing $\overline{F1}$ = 0 and M1 to be on, and thus allowing output F1 to closely follow the power clock PCK waveform. In the next clock period B, the auxiliary clock CX = 0 disables the logic evaluation. The previously stored logic state repeats at the outputs F1 and $\overline{F1}$, regardless of the inputs, so that the stage that follows can perform logic evaluation.

In a system of these circuits, all logic stages are supplied by the same power clock PCK. The logic evaluation is enabled in alternate logic stages by the auxiliary clock CX and its complement $\overline{CX}$. Because of the memory function, pipelining is inherent, as in other memory-based adiabatic schemes. The auxiliary clocks drive only MOS transistor gates so that the additional energy loss can be minimized by reducing the clock amplitudes, or by using a high-efficiency resonant clock scheme. The overhead loss is relatively small, especially when more complex logic functions are implemented in the logic trees. Since this logic operates with a single power clock, a very simple, power- and area-efficient power clock generator can be applied. The low-power auxiliary clock signals can be distributed using the same techniques used in conventional clocked CMOS. Therefore, power and clock distribution are simpler and more efficient using this single power clock plus auxiliary control clock scheme than possible in multi-phase power clock adiabatic logic families.

Example Power Clock Generator for Low-Energy Logic Low-energy logic presents a capacitive load to the power clock generator. One approach to power clock design is to integrate all power clock switching transistors and associated control circuitry on the same CMOS chip with the low-energy logic. Thus, only a small resonant inductor is added as an external component. The power may be supplied from a battery.

The simple power clock generator considered here is the 1N single-phase generator shown in Figure 3. The generator consists of a single NMOS active device Q (hence "1N") in parallel with the logic, and a single resonant-tank inductor L_r in series with the (VDD/2)-valued dc source. The externally applied clock signal CK has period (1/fc) and amplitude V_G as shown in Figure 3. Optimum V_G for minimum energy dissipation can be found to be $2V_t$ [8]. As shown in Figure 3 the low-energy logic is represented by an approximate lumped-element model which includes an equivalent capacitor C to model the energy storage in series with a resistor R to model the losses. The clock frequency is approximately the resonant frequency of the L_rC circuit.

Transistor Q is turned on for a brief interval $t_{on} = D/f_c$ in each period of externally applied clock CK, only for the purpose of adding energy to the L_rC resonant tank to make up for losses during the previous cycle. The turn-on occurs when the power clock is at zero volts. The switch duty ratio D can be controlled to regulate the power clock amplitude (which is ideally equal to VDD) if the available dc voltage is not well regulated, or to compensate for load variations caused by changes in logic activity. In [8] optimum

dimensions of switching device Q are derived.

Adiabatic Logic and Power Clock Integration. Shown in Figure 4 within the dotted line indicating the boundary between on- and off-chip components are a cascade of single power clock logic functions, the power clock's switching transistor and a flip-flop to generate the necessary auxiliary clock signals CX and $\overline{CX}$. The dc source is VDD/2. The auxiliary clocks CX and $\overline{CX}$ are obtained easily from the gate drive signal CK for the switch Q in the power clock generator. Both the gate drive and the auxiliary clocks are O-to-VDD/2 square waves. In [8], the gate-drive amplitude (1.5V) is very close to the optimum ($2V_t$) value.

In a simulation of the system in Figure 4 [8] with VDD=3v, a clock frequency of 20MHz, the total energy loss at this clock frequency is 42fJ per stage, where 29fJ (69%) is the logic loss, 10fJ (24%) is the loss in auxiliary clocks, and 3fJ (7%) is lost by the power clock generator [8].

Considerations for Adiabatic Multiple Valued Logic Circuits

Manipulations of voltages, currents, and charge are what designers of Multiple Valued Logic circuits use to create the desired multiple valued output signals from the binary and multiple valued input signals. Nearly every circuit design requires that multiple valued input and intermediate signals be evaluated by comparison to some known thresholds that may represent logical, arithmetic, or identification functions. The results of these threshold comparisons reveal characteristics of the evaluated signal that are then used to create the desired multiple valued output signal that correctly represents the desired identification, logical, or arithmetic operation that is to be performed. Threshold comparison is usually a binary decision, or a combination of binary decisions. From the discussions above, it is apparent that memory schemes for binary adiabatic logic can be directly applied to the realization of multiple valued adiabatic logic if we make use of the binary results of threshold comparisons. Thus, multiple valued adiabatic logic can use a single phase power clock and an auxiliary control clock to excite all MVL logic blocks as discussed above. Pipelined propagation of signals down a cascade of MVL adiabatic logic functions would be accomplished by using alternating phases of an auxiliary control clock and its binary complement. Adiabatic MVL circuits based upon the idea of latching binary comparator decisions within the MVL function are discussed below.

We have been attempting to develop a multiple-valued-memory-based scheme for adiabatic MVL but we have not yet found a satisfactory solution. We had hoped to coalesce the auxiliary clock and additional logical and control circuitry into simple MVL memory circuits, examples of which appear in [9, 10], and produce elegantly simple adiabatic versions of MVL circuits. The problem encountered trying to use a voltage-mode MVL latch similar to those in [10] as the memory element that corresponds to the cross-coupled pair of inverters in the binary design is that these MVL memory circuits are based upon the comparison of MVL voltage signals to multiple fixed voltage references. Consider the hold interval in which the logical value of the output is to stay fixed while the inputs are allowed to change. If we allow the global power clock voltage to go to zero during the hold interval (when the present output is used to recreate itself), we will lose the reference signals, the information in the outputs of the threshold comparators (unless they are latched as described above and later), and as a result the value of the output. When the power clock is restored to the level at which the correct references are created we have lost the information about the value of the output and cannot recreate it. This prevents the use of simple alternate evaluate and hold intervals of the auxiliary clock in these voltage-mode MVL memory circuit. Similar arguments apply to current-mode and charge-mode MVL circuits. Although complicated approaches for realizing MVL-memory-based adiabatic MVL circuitry are being examined that use multiple phase power clocks, or multiple auxiliary control clocks, or a combination of fixed VDD and power clock, none are considered any better than the approach described below. The following approach uses the memory-based adiabatic binary logic memory circuit described above to hold the binary results of voltage threshold comparisons within an MVL function, but this approach does not use MVL memory directly. We consider this approach a good starting point and continue to study alternatives and improvements.

We could realize an adiabatic latched version of nearly any MVL function by putting the latch-pair of cross-coupled inverters on appropriate threshold comparators and introducing a latch control clock. For example, a quaternary threshold logic full adder, which creates the 2-quaternary digit output, base-4 count of the sum of the 2 quaternary inputs and the binary carry input, is often realized with 7 threshold comparators. An adiabatic version of the quaternary full adder could be realized by putting the cross-coupled inverter latch pair and logic-control trees on each of the MVL circuit's threshold comparators. The comparators are allowed to react to their multiple valued input during the follow mode of the clock, and the comparator outputs are latched during the hold clock interval. Thus, during the hold clock interval the MVL circuitry that is driven by the comparator outputs creates the appropriate MVL outputs to realize the desired MVL function.

Since the power clock, auxiliary clock, and internal circuit waveforms are complicated, the simple quaternary latch [9, 10] is used here to illustrate the adiabatic operation of an MVL circuit. A quaternary latch [9, 10] as shown in Figure 5 uses a clock-controlled switch pair to direct either the quaternary input or the recreated quaternary output (Q) of the quantizer to the input of the quantizer. The quantizer decodes the quaternary input signal into an equivalent pair of binary signals as shown in Figure 6 that are then re-encoded into an output that is the same quaternary logical value as shown in Figure 7. This recreated quaternary signal is fed back to the input of the clock-controlled switch pair. During the follow clock mode, the quantizer acts upon the input and regenerates the quaternary value at its output, Q. During the hold clock mode, the input is disconnected from the quantizer but the positive feedback of quantizer output Q to the

quantizer input holds the quaternary value of Q. To realize an adiabatic quaternary latch, we place an adiabatic latch as shown in Figure 2 on each of the 3 threshold comparators, and remove the clock controlled switch pair that directs either the input or output to the quantizer. Since each comparator is latched, the quaternary feedback signal is not needed.

By latching the 3 comparators, shown in Figure 6 with references "low", "middle", and "high", we remove the requirement for the clock controlled transmission gate in Figure 5 that routes the input signal or the feedback signal into the quantizer. With clocked latches on the 3 comparator signals developed within the quantizer, we retain the normal latch function, can create quaternary outputs during the hold clock interval, and also allow the use of the adiabatic power clock. SPICE simulation waveforms for such a realization of an adiabatic MVL latch are shown in Figure 8. The top trace is the 5V power clock, PCK, the second trace is the 5V auxiliary clock, CLK, the 3rd trace is the (0V, 1.67V, 3.33V, 5V) quaternary input, the 4th and 5th traces are the 5V MSB and LSB generated by the circuitry in Figure 6 using PCK for power instead of a constant VDD = 5 volts, and the 6th trace is the (0V, 1.67V, 3.33V, 5V) quaternary output generated by the circuitry in Figure 7 using PCK for power instead of a constant VDD = 5 volts. In Figure 8 the simulations show that the MSB, LSB, and Qout take the correct values during the follow and hold intervals of the auxiliary clock. Thus, these preliminary results indicate that the realization of a memory-based adiabatic MVL circuit appears to be possible. Simulation studies continue. These and other circuits have been submitted for fabrication in a 2-micron nwell CMOS technology. Experimental results are expected soon.

Conclusion

Low-energy, adiabatic binary and multiple valued CMOS logic have the potential of significantly reducing the energy consumption of digital VLSI chips. In this paper we summarized concepts of adiabatic binary CMOS logic design, and addressed considerations for application of these techniques to adiabatic MVL design. A simple example of an adiabatic MVL circuit was presented.

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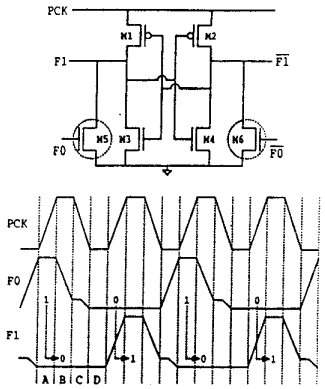

Figure 1 Inverter in the logic family of [6]

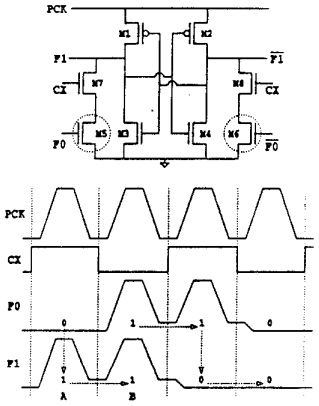

Figure 2 Inverter in clocked adiabatic logic

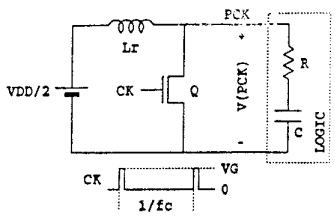

Figure 3 1N single-phase power clock generator

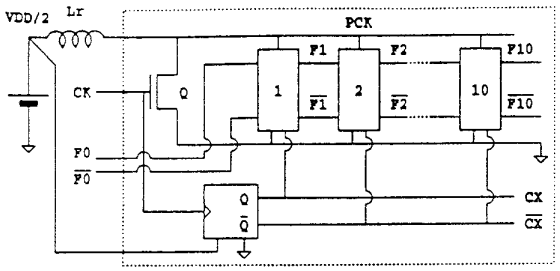

Figure 4 1N power clock generator integrated with a chain of inverters

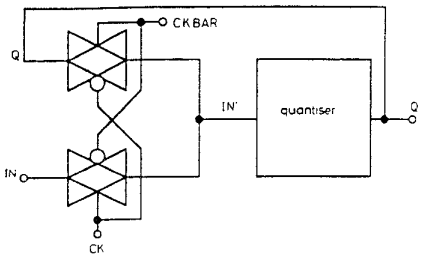

Figure 5 MVL latch block diagram

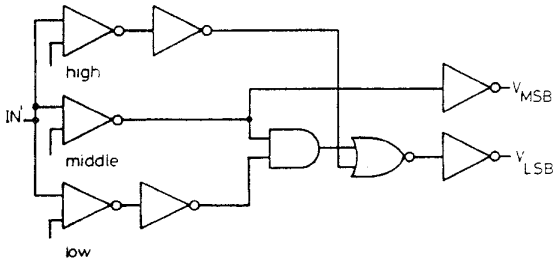

Figure 6 Comparator and logic section of quaternary latch quantizer

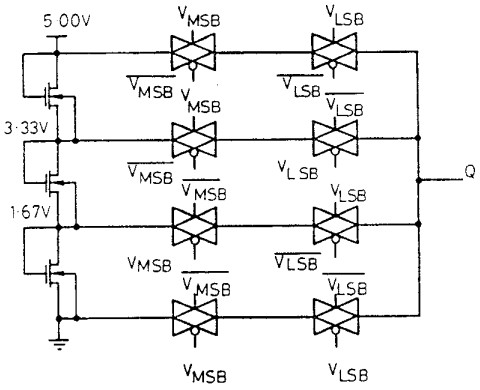

Figure 7 Logic-level regeneration and output section of quaternary latch quantizer

Figure 8 Adiabatic Quaternary Latch Waveforms