CLOCKED CMOS ADIABATIC LOGIC
WITH SINGLE AC POWER SUPPLY

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ABSTRACT *This paper describes a low-power clocked CMOS adiabatic logic (CAL) with only one ac power supply that serves as the power clock. Each CAL stage performs true and complementary logic functions, and presents a constant capacitive load to the power clock generator. A simple and efficient resonant power clock is integrated with the logic to generate the required ac supply waveform and facilitate adiabatic energy transfers. Energy savings comparable to adiabatic logic families that require multi-phase power clocks have been verified by simulation tests of the CAL supplied by the integrated power clock generator.*

I – INTRODUCTION

Power consumption is a fundamental constraint in both high-performance and portable, energy-limited systems. Circuit-level adiabatic techniques have been proposed to reduce energy losses in CMOS logic. The techniques are based on slowing down energy transfers and recovering energy from the logic. Although logic with asymptotically zero energy loss is feasible [1], schemes with partial energy recovery [2]-[6] would be preferred because of much simpler and area-efficient implementation.

Instead of dc supply voltage, all types of adiabatic logic families require ac power supply voltage waveform(s) that also serve as clock(s) for the logic. Most adiabatic schemes require four phase-shifted power clock waveforms for correct stage-to-stage interface [5, 6]. The problem of efficiently generating and distributing the four power clocks clearly becomes a limiting factor. An exception is the recovered-energy logic [3], where only one power clock is required. However, this logic is based on bipolar implementation, allows only simple logic functions per stage, and has relatively low noise margins.

In this paper we describe a CMOS adiabatic logic that operates with a single power clock. In addition, we show how a simple and efficient resonant power clock generator can be integrated with the logic.

II – CLOCKED ADIABATIC LOGIC

The inverter stage of the *clocked adiabatic logic* (CAL) is shown in Fig. 1. The cross-coupled $M1 - M4$ provide memory function. The circled devices $M5$, $M6$ can be replaced with nmos logic trees to perform more complex complementary logic functions on the true ($F0$) and the complementary ($\overline{F0}$) logic inputs. The CAL stage topology is a modification of the adiabatic logic proposed by Denker [6], with the clocked *enable* devices $M7$, $M8$ added in series with the logic trees. The purpose of the modification is to allow operation with a single power clock PCK. The CAL timing differs significantly from the logic proposed in [6].

Idealized CAL timing waveforms are shown in Fig. 1. The power clock PCK is shown as a 0 to V_{DD} trapezoidal waveform. In the clock period A, the auxiliary clock CX enables the logic evaluation. For $F0 = 0$, $M8$ and $M6$ are on, $\overline{F1} = 0$, $M1$ is on, and the output $F1$ closely follows the power clock waveform. In the next clock period B, the auxiliary clock CX = 0 disables the logic evaluation. The previously stored logic state is repeated at the outputs $F1$ and $\overline{F1}$, regardless of the inputs, so that the stage that follows can perform logic evaluation.

Idealized timing waveforms in a chain of logic stages are shown in Fig. 2. The same power clock supplies all CAL stages. The logic evaluation is enabled in alternate logic stages by the auxiliary clock CX and its complement $\overline{CX}$. Because of the memory function, pipelining is inherent.

III – POWER CLOCK AND AUXILIARY CLOCKS

Fig. 2 shows implementation of the power clock with a single nmos device Q *in parallel* with the logic. The device Q is turned on during a small fraction of the clock period at the point when PCK ≈ 0 and auxiliary clocks change states. The energy is added to sustain the oscillation in the resonant circuit formed by the small external inductance L and the equivalent logic capacitance C. With both true and complementary logic functions in each stage, the capacitive load is independent of the logic states. From a low-voltage dc power source $V_{DD}/2$, the power clock PCK is generated as an approximately sinusoidal waveform with amplitude $V_{DD}/2$, and with a dc offset equal to $V_{DD}/2$ [7].

The device Q, and the enable devices in the CAL are driven by reduced-amplitude, 0 to $V_{DD}/2$ square-wave signals. The overhead loss in the low-power non-adiabatic clocks is relatively small, especially when more complex logic functions are implemented in CAL stages. The auxiliary clocks CX and $\overline{CX}$ are obtained easily from the clock CK for Q,

which sets the system clock frequency f_c, as shown in Fig. 2.

IV – SIMULATION RESULTS

A chain of inverters with the power clock generator, as shown in Fig. 2, has been tested by simulation using a 0.8μ CMOS technology and $V_{DD} = 3V$. Table 1. shows the total energy loss W, relative to CV_{DD}^2 of plain CMOS, as a function of the power-clock frequency f_c. Fig. 3 shows the waveforms obtained at $f_c = 20MHz$. The total energy loss at this clock frequency is $W = 42fJ$ per stage, where 29fJ (69%) is the logic loss, 10fJ (24%) is the loss in auxiliary clocks, and 3fJ (7%) is lost by the power clock generator.

CONCLUSION

The proposed clocked adiabatic logic (CAL) operates with a single ac power clock and a pair of low-power, reduced-amplitude auxiliary clocks. It offers energy savings comparable to other adiabatic logic families, but with much simpler and more efficient power distribution. The power clock generator integrated with CAL has a single active device and accounts for only 7% of the total energy losses.

References

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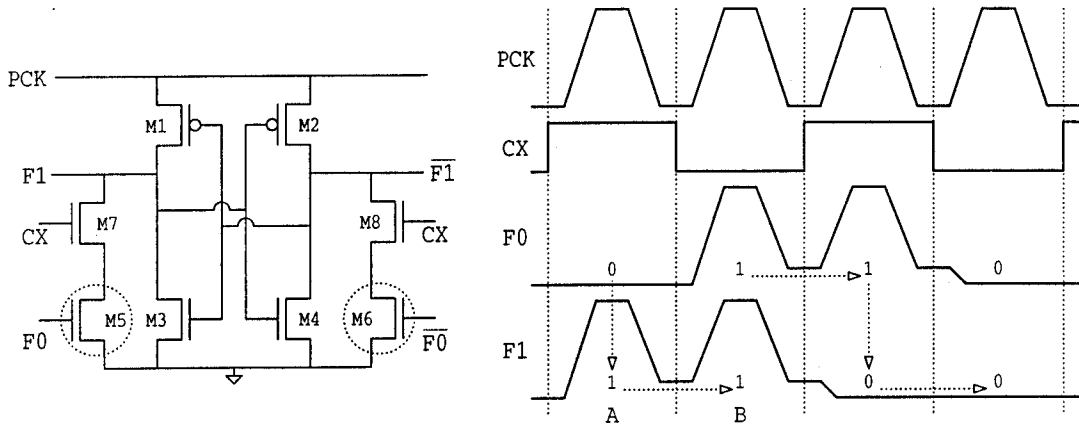
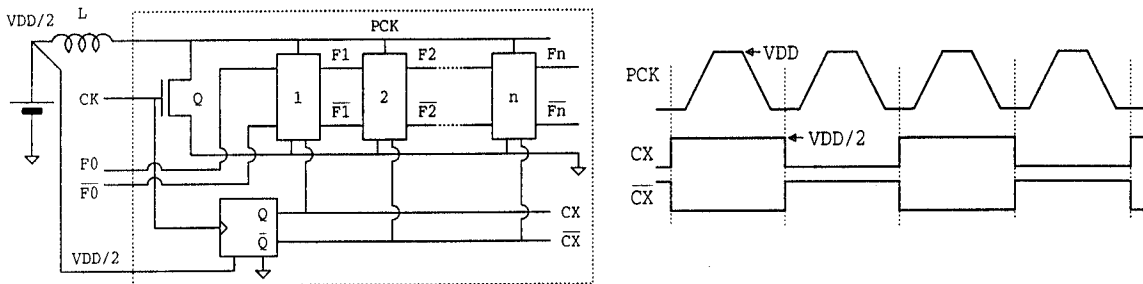Figure 1: CAL inverter with timing waveforms.

Figure 2: A chain of CAL logic gates with integrated power clock generator and system waveforms.

f_c[MHz]	10	20	30	40	50	60	80	100	120
$W/(CV_{DD}^2)$ [%]	11.4	12.7	14.2	16.0	17.9	19.7	23.4	28.6	37.9

Table 1: Total CAL energy loss W (logic, power clock, and auxiliary clocks), per power-clock period, relative to CV_{DD}^2, as a function of the power-clock frequency f_c.
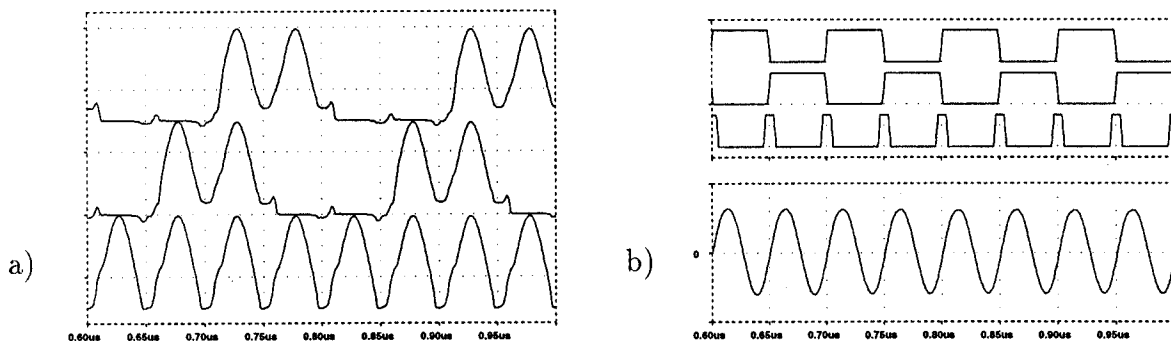

Figure 3: Simulation results for a chain of 10 CAL inverters with the integrated power clock generator at $f_c = 20$MHz. a) top to bottom: F_9, F_{10}, PCK, all at 2V/div; b) top to bottom: CX, $\overline{\text{CX}}$, CK, all at 2V/div, $i(L)$ at 100μA/div.