PASS-TRANSISTOR LOGIC FAMILY FOR HIGH-SPEED AND LOW POWER CMOS

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ABSTRACT

This paper presents new pass-transistor logic named DVL which containing fewer transistors than DPL and achieving better performance. In comparison with conventional CMOS, DVL shows performance improvement of up to 43% while the improvement in size ranges around 20%. In comparison with DPL circuits, there is 15% to 50% improvement in speed, and in comparison with CPL (using lean cells) there is a 10% improvement. As far as the power consumption is concerned comparison between DVL and the Conventional CMOS shows a 30% to 50% savings in favor of DVL. A method for synthesis of such networks is also developed and demonstrated. This new logic has advantages over CMOS and is characterized by excellent speed and low power.

1. INTRODUCTION

New logic CMOS families using pass-transistor circuit techniques have recently been proposed with the objective of improving speed and power consumption [4-6,8]. Two of them, simultaneously developed by Hitachi CPL [4] and DPL [6], are the most notable. The Double Pass-Transistor Logic, developed by Hitachi in 1993 demonstrated an 1.5nS 32-bit ALU in 0.25 μm CMOS technology [6] and 4.4nS 54X54 bit multiplier [9]. However, DPL has not yet been fully adopted because of its use of p-type transistors. CPL has been advantageous because it uses only n-type transistors, however it suffers from the problem of the threshold voltage drop at the output. The objective of this work is to develop a new logic family and the synthesis method for pass-transistor logic which will minimize the number of transistors used in DPL and yet preserve the speed of the logic. We used 1-μm CMOS technology (available to us) to test our examples and make comparisons with DPL.

2. NEW LOGIC FAMILY: DVL

The new logic family was obtained from DPL by elimination of the redundant branches and rearrangement of signals. This simplifications still preserves full swing operation of DPL and improves the speed. The speed improvement is a direct result of elimination of one branch containing one transistor. This minimizes the capacitive load "seen" by the previous gate by minimizing the number of inputs and number of capacitive loads.

The new logic family termed DVL (Dual Value Logic) is achieved in two steps:

(a) elimination of redundant branches in DPL

(b) elimination of branches via signal rearrangement

(c) combination of (a) and (b) using two better halves

The process in which redundant branches are eliminated (a) is illustrated in Fig.1.

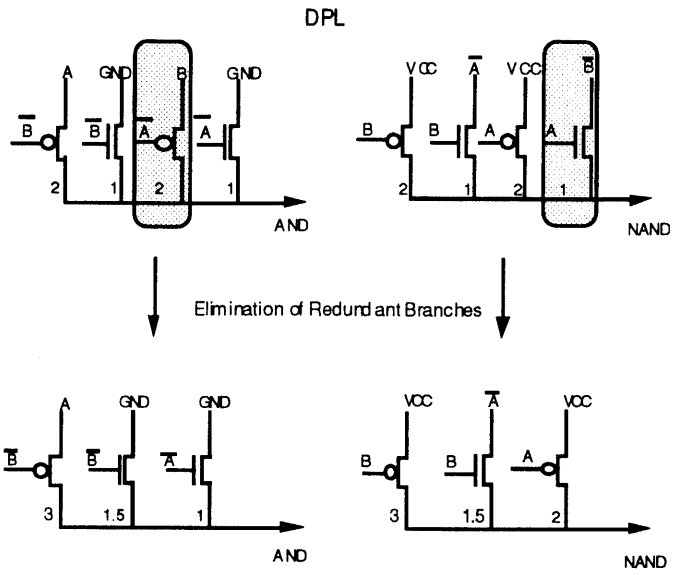

Fig. 1. *Elimination of Redundant Paths*

The simplification process is illustrated in Fig. 2.

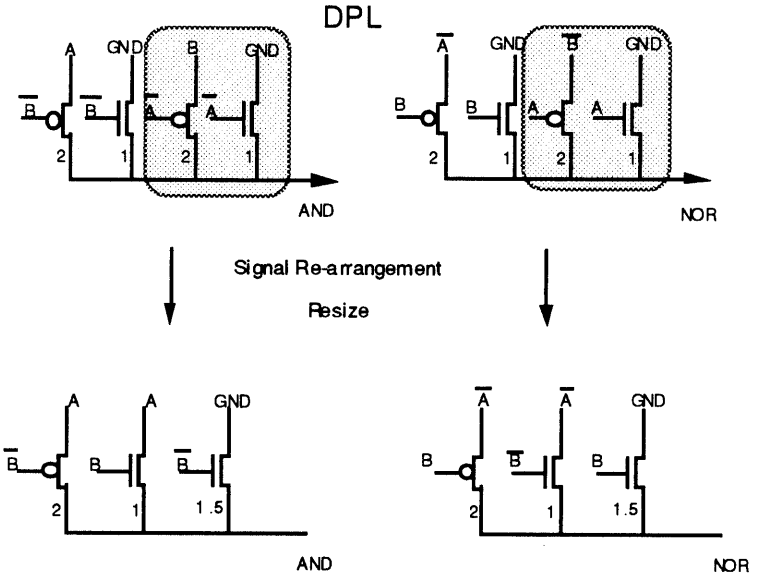

Fig. 2. *Signal Re-arrangement*

Finally (c), we have chosen a faster half from (a) and form (b). Fortunately (a) produces a faster NAND while (b) produces a faster AND which makes a complete gate shown in Fig.3. We named it DVL (Dual Value Logic). The resulting DVL gate contains total of 8 transistors (3 p-transistors and 3 n-transistors) compared to DPL consisting of 4 transistors of each type. There is total of 9 inputs in DVL versus 12 in DPL resulting in a smaller capacitive load of DVL gate. Of those inputs 3 are connected to the transistor source and 6 to the gate (3 to p-type and 3 to n-type). (in DPL 4 are connected to the source 4 to p-type and 4 to n-type transistors). The total area (taking resizing into account) is only 5% larger in DVL gate. The speed advantage is 20% in favor of DVL.

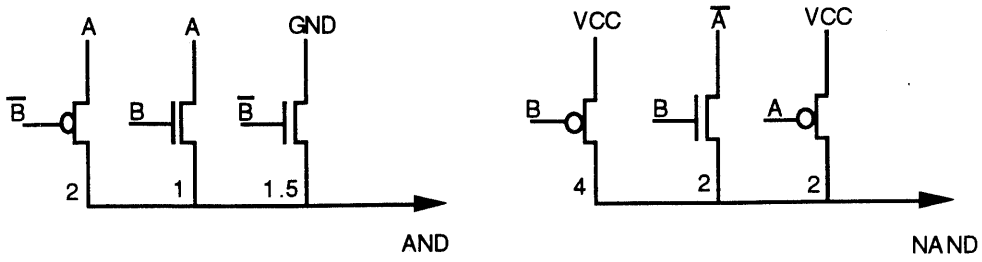

Fig. 3. *Resulting DVL gate*

In summary, the comparison between NAND/AND DPL gate and NAND/AND DVL shows:

- 20% speed improvement, utilizing 75% of the transistors used in DPL.
- 25% less connections and wires as compared to a DPL gate.
- The 4% area increase in comparison to DPL is not found to be substantial.

Similar method can be used to build the NOR/OR gates.

3. DVL SYNTHESIS METHOD

In this work we developed a method for synthesis of DVL based on transistors instead of logic gates. In place of conjointly assembling several basic gates, functions are synthesized at the transistor level. In addition, a programming of this method has been developed to prove its efficiency.

The key point of DVL synthesis consists of employing Karnaugh-Map at the transistor level. Thus, we are not cascading several logic gates in order to implement a given function. Instead we are building functions by directly using several transistor levels in series. A "pseudo Karnaugh-Map" is used when the number of inputs was less than 8 because its explanation is simple. A "pseudo Quine McCluskey" technique has been programmed instead.

3.2. DVL Synthesis Rules

The rules for synthesis of DVL circuits are described here and illustrated in Fig.6.

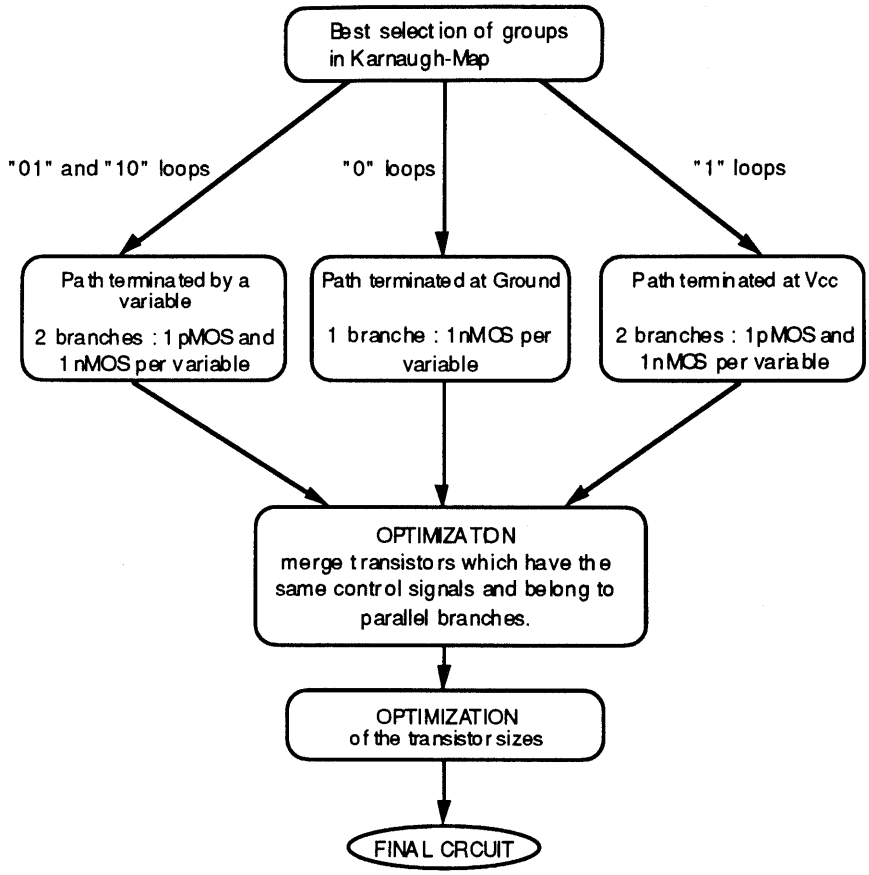

Fig. 6. *DVL Synthesis Rules*

4. RESULTS

4.1. Comparison with conventional CMOS

An example showing a function produced in DVL and conventional CMOS is shown in Fig. 9. This Figure also illustrates the basic differences in how are those circuits obtained. It is noticeable that the length of the pass-transistor chain is shorter in DVL than in conventional CMOS. Also instead of terminating at VCC and GND the chains in DVL terminate at the input variables. This has its power advantages resulting in charge being "passed" and used in the next stage, rather than being dissipated at one of the terminal nodes (VCC or GND).

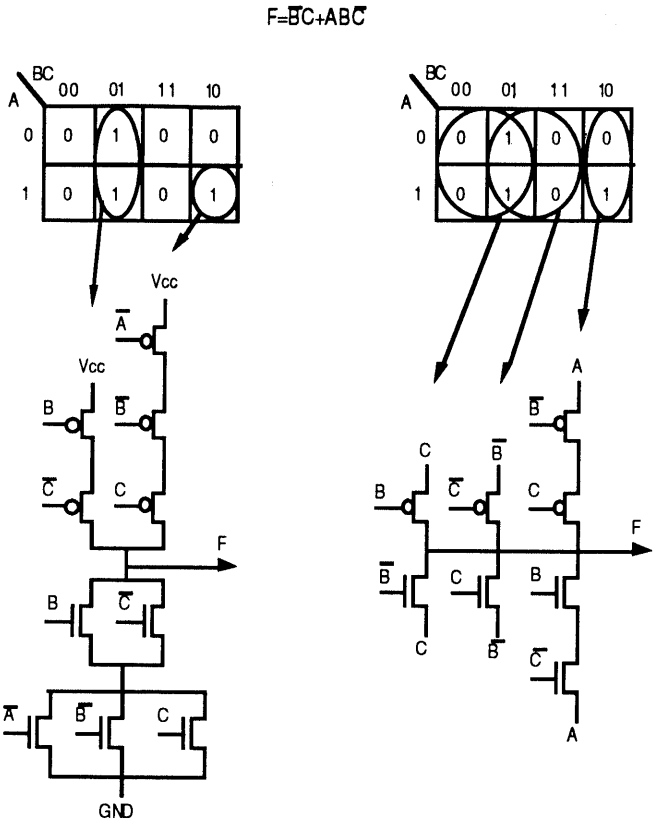

Fig. 9. *Example ($F=\bar{B}C+AB\bar{C}$) comparing DVL and conventional CMOS*

A comparison between DVL and conventional CMOS is given in Fig. 10. The improvement in the global size, the number of transistors and the delay of the circuit is shown.

Function F	CMOS synthesis	DVL synthesis	Savings
# of transistors	10 nMOS 10 pMOS	8 pMOS 8 nMOS	20%
# of levels	3 levels of gates	2 levels of transistors	
Global size of gate	44	36	18%
Delays using buffers at 50% of the supply voltage value	430ps	245ps	43%
Ratio of transistor geometries	wp/wn = 2	wp/wn = 2	

Fig. 10. *Comparison between DVL and conventional CMOS*

The simulation results are shown in Fig. 11. showing the output waveforms at the output of the given function F.

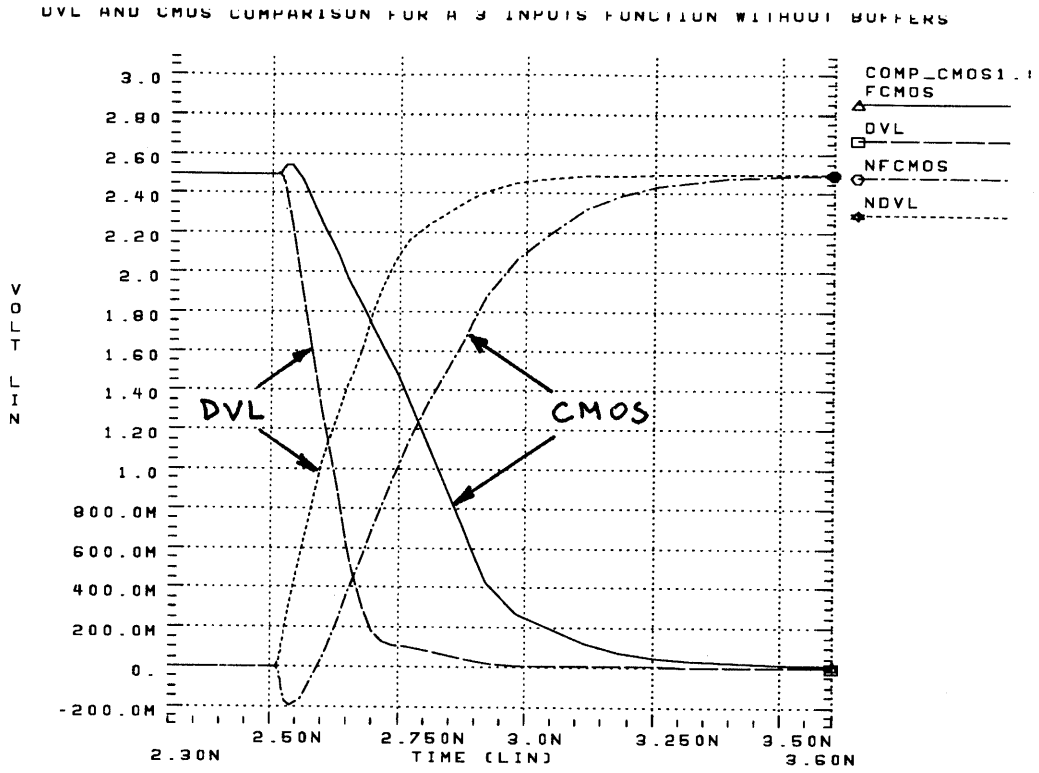

Fig. 11. *Delay Comparison between DVL and Conventional CMOS for a 3 inputs function F*

CONCLUSION

In this work DVL logic family has been developed. This logic has advantages over standard CMOS as well as new pass-transistor families such as DPL and CPL. The improvement over DPL is in 25% less transistors with the advantages of decreasing the number of connections and wires. The second advantage involves the method developed to automatically build DVL logic. Instead of using common method in which circuits are synthesized at the gate level, DVL synthesis generates circuits directly at the transistor level. The advantages of DVL synthesis lay in the three main domains : Area, Speed and Power consumption. In each case, the global size of transistors used in DVL was smaller compared to other circuits. In comparison with conventional CMOS, DVL shows performance improvement of up to 43% while the improvement in size ranges around 20%. In comparison with DPL circuits, there is 15% to 50% improvement in speed, and in comparison with CPL (using lean cells) there is a 10% improvement. However, the exact speed improvement is dependent on each particular circuit. As far as the power consumption is concerned comparison between DVL and the Conventional CMOS shows a 30% to 50% savings in favor of DVL. Generation of DVL is supported by an automated synthesis tool based on the algorithm developed in the course of this work.

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