An ECL Gate with Improved Speed and Low Power in a BiCMOS Process

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Abstract—**An emitter-coupled logic (ECL) gate exhibiting an improved speed-power product over the circuits presented in the past [1], [7]–[11] is described. The improvement is due to a combination of a push–pull output stage driven by a controlled current source, thus reducing the static and increasing the dynamic current. This circuit has better driving capabilities and improved speed, yet it uses an order of magnitude less power than a regular ECL gate. Due to its reduced power consumption, this gate allows for a higher level of integration of ECL logic. The realization of this circuit using a regular bipolar process is also possible.**

I. Introduction

With the increase in demand for high-performance servers in the mid-range computer family, emitter-coupled logic (ECL) technology has gained new attention [3]. In part, this is due to its ability to achieve higher levels of integration, due to technological improvements, as well improvements in cooling techniques. Development of new ECL circuits characterized with much lower power consumption than regular ECL had its impact as well. Another area where ECL circuits are very attractive is the clock generation and distribution part of the chip. Recent advances in design for low power have demonstrated the use of a half-swing clocking scheme in reducing the power of the clock distribution network [5]. Such a network could make very good use of the ECL circuits treated in this paper.

Some useful ECL parameters and a discussion of ECL technology are given in [1], while a survey of recent advances in ECL circuits is given in [7]. Comparison of ECL with CMOS technology with respect to future trends is given in [2]. Several new ECL configurations have been developed since then with the aim of reducing the ECL power and increasing the speed [11], [12]. In all of the cases, it is essential to reduce the power consumed by the ECL circuit and yet maintain the driving capabilities and switching speed.

There are two inherent advantages of using ECL over CMOS:

1) Switching current in a bipolar differential pair is much faster than changing the voltage at the MOS transistor terminals. This advantage is applicable to the part that performs the logic operation.

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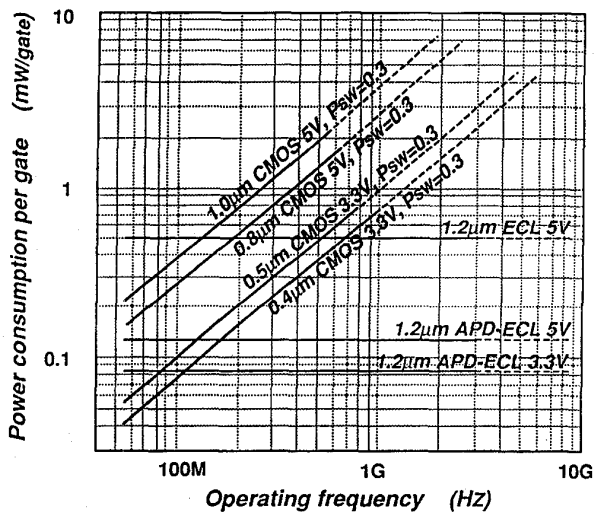


Fig. 1. ECL-CMOS speed-power trade-off (as taken from [6]).

2) The output voltage swing, which is the swing of the signal required to propagate through the interconnection, is much smaller than in a comparable CMOS structure. This is of a particular importance today when the cycle time is becoming so short that the signal propagation time in the interconnections becomes comparable to the cycle.

The reduced voltage swing helps in reducing the propagation delay as well as power given that at the dynamic portion of the power consumed in the chip is

$$P_0 = f_0 \times C_L \times V_S^2.$$

At very high frequencies of operation (above 100–200 MHz), the power consumption of CMOS can be quite substantial. A dynamic portion of power (which increases linearly with frequency) starts to dominate. Some recently introduced CMOS processors are consuming amounts of power that are in the same order of ECL power [4]. Therefore it is a common misunderstanding to think of CMOS as low power technology in the high-performance domain. This observation is illustrated very well in a chart provided by Kuroda [6] and shown in Fig. 1.

The ECL power depends on the frequency of operation as well. However, this dependency is not as strong as it is in the case of CMOS. The reason for it is that the voltage swing in ECL is an order of magnitude smaller, thus making

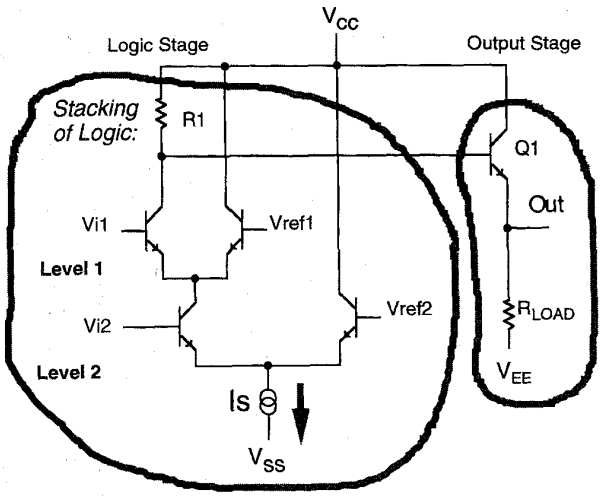


Fig. 2. Structure of a regular ECL gate.

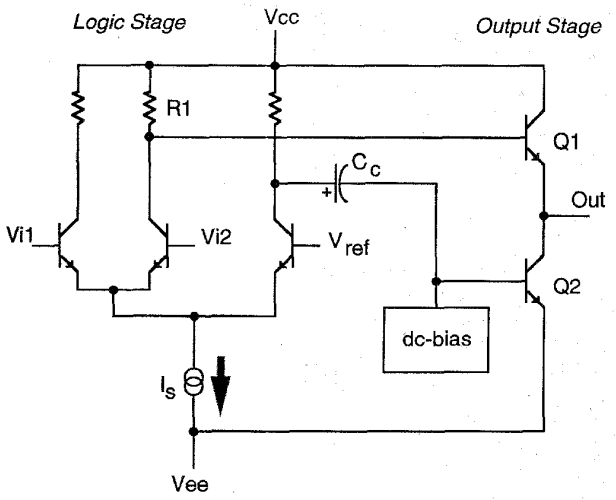


Fig. 3. APD-ECL from IBM [8].

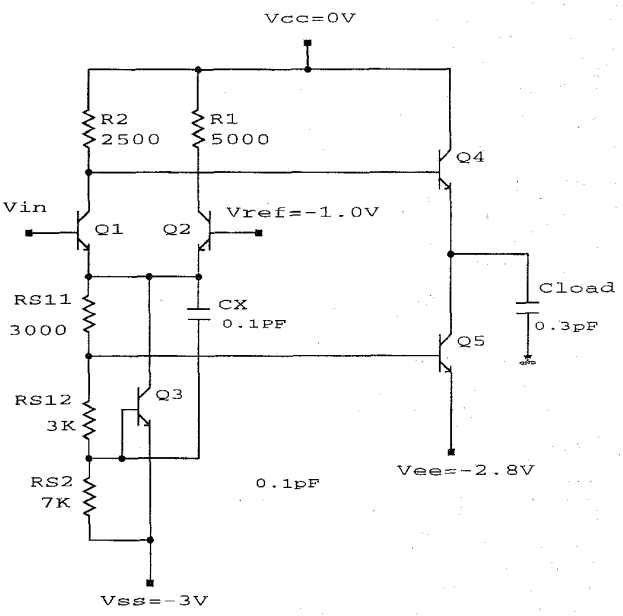


Fig. 4. AC-APD-ECL from IBM [10].

this dependency factor $(C_L \times V_S{}^2)$ two orders of magnitude smaller.

A very important part of an ECL gate is its driving stage because in the driving stage most of the power is used to provide sufficient signal driving capability. The speed of the gate depends on how much dynamic current the output drive stage provides.

In a regular ECL gate (Fig. 2), the switching speed is very much dependent on the value of the resistor R_{LOAD} in the path to V_{EE} [1]. This creates a direct relation between the static and dynamic current in the output stage. This resistor should be small, preferably, in order to rapidly discharge the load capacitance. However, when the output voltage is at the *high* level the current thorough R_{LOAD} can be substantial, thus amounting to substantial static power of the gate. Any increase in the dynamic current results in increased static power. To achieve rapid changes of the output voltage the output transistor has to be driven with the substantial current from the logic state (about five times due to degradation of β in that region). Consequently, any desired increase in speed is paid for by the substantial static power consumed by the gate.

Authors from IBM developed several ECL structures using active-pull down (APD) bipolar combination in the output APD-ECL [7]–[10]. The operation of IBM's APD-ECL [8] is illustrated in Fig. 3. A review of those techniques is given in [7] describes various structures in which a connection exists from the logic tree of the ECL structure to the "*pull-down*" output transistor which causes an extra amount of charge to be injected into the base of the "*pull-down*" transistor Q_2, thus speeding up the transition. Their circuit results in faster operation at lower power, compared to regular ECL.

Another refinement of the APD-ECL family developed by the same authors are the AC-APD-ECL [9] and the AC-CS-APD-ECL circuits [10], the latter being slightly faster [9]. Despite its remarkable performance, the AC-CS-APD-ECL has some shortcomings. The operating point of the output stage in AC-APD-ECL depends on the operating point of its logic stage. This dependency makes adjustments in the logic stage difficult, especially if one is trying to reduce power. Any adjustment of the operating point related to power involves both logic and output stages, which makes this process rather difficult. AC-CS-APD-ECL circuit is shown in Fig. 4. It is also difficult to cascode the logic higher than one level (cascoding is illustrated in Fig. 2). The emitter-dotting operation is not permitted either.

Recently, several other very effective ECL circuits were reported [11], [12], [15], most notably the circuit developed by H. J. Shin of IBM named FPD-EF-ECL [11]. This circuit has a remarkable simplicity (as shown in Fig. 5), while yielding several benefits such as the ability to permit emitter dotting. However, those schemes were not able to significantly reduce the static current in the output stage, which also affected the driving capability and in turn the speed of the gate.

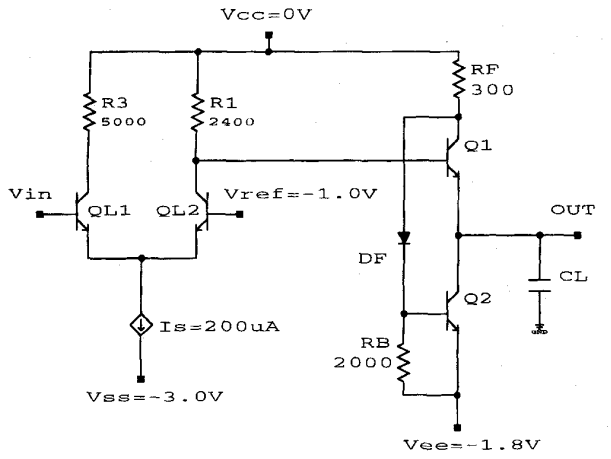


Fig. 5. FDP-EF-ECL from IBM [11].

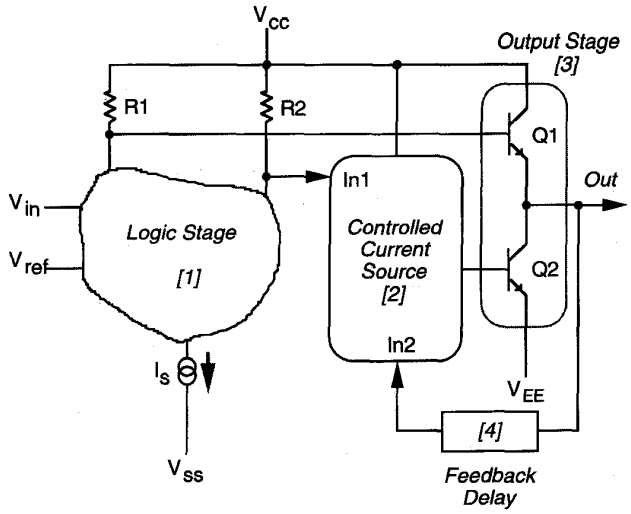


Fig. 6. FCCS-APD-ECL circuit operation.

Our objective was to develop an ECL circuit with improved driving capabilities which will result in faster operation and lower sensitivity to loading (increased fan-out capabilities). Yet, our objective was to design a gate with lower power compared to the previous work [7]–[12].

II. Circuit Operation

We have developed a new circuit which utilizes feedback-controlled-current-source in an active-pull-down ECL configuration (FCCS-APD-ECL) [13], [14]. Conceptual operation of this circuit is summarized in Fig. 6, which illustrates the major parts of this circuit. The circuits consists of an ECL logic tree [1], controlled current source [2], output driver stage [3], (consisting of the transistors Q_1 and Q_2) and feedback stage [4]. The current in the current source is controlled by the state of the logic stage as well as the output state (via the feedback stage).

The controlled current source (CCS) injects current into the pull-down transistor in the output stage during transition periods. In a steady-state, the current in Q_2 is reduced to its minimum value. Resulting circuit realization has a better power-delay product than ones previously reported [1], [7]–[11] because its output stage is operating in a truly push-pull mode of operation. The power consumed in the output stage is an order of magnitude lower than in its counterparts yet maintains comparable speed. The ability to drive large capacitive loads is substantially improved.

A. Operation

The circuit described in this paper uses a separate power supply in the output stage, electrically separating the logic stage from the output stage. There are several benefits resulting from this configuration

a) The logic stage is decoupled from the noise which is usually generated in the output stage.
b) The operating point of the output stage is not dependent on the logic stage, therefore the logic can be cascoded in more than one level, thus allowing for more complex logic operations within one ECL tree. This is not possible in AC-CS-APD-ECL [10].
c) Reduced power supply voltage in the output stage results in an overall power reduction, given that the output stage is a main contributor to the power budget.

The current is injected into the base of Q_2 only when: the output is *high* and the voltage at the opposite end of the logic stage R_2 becomes *high*. It is obvious that this can happen only at the beginning of the transition from *high* to *low* when the current I_s in the logic stage is switched from R_2 to R_1 branch. Once the output reaches *low*, the current injected into the base of Q_2 will be cut-off (reduced).

During the logic *low* at the output, there is no current in Q_2 and the circuit is ready for the transition from *low* to *high*, which will occur when the current I_s is switched from R_1 to R_2 branch. This transition enables Q_1 to drive the output *high* while the voltage drop across R_2 will prevent the CCS from supplying the current to the base of Q_2. The behavior of the CCS can be summarized as:

i) The current source is producing its maximal available current during the *high*-to-*low* transition of its output stage.
ii) During the *low* to *high* transition, as well as in the steady state (low or high) the current source is in the reduced current mode providing just enough current to keep the transistor in slightly conducting mode.

High current injected by the CCS (2) into the output transistor Q_2 ensures sufficient current drive for the output transistor Q_2 to rapidly discharge the load capacitance C_L and drive the output node from *high* to *low* state. Output transistor Q_1 is driven directly from the logic stage. The current in the CCS is controlled by the logic stage (1) and it is in the opposite phase of the current driving the output transistor Q_1. This assures that the transistors Q_1 and Q_2 are driven in opposite phases thus eliminating direct current path from V_{cc} to V_{EE}.

In summary, *low* to *high* transition of the output stage is produced by driving Q_1. The output node will assume *high* value and after a reasonable delay through the feedback path

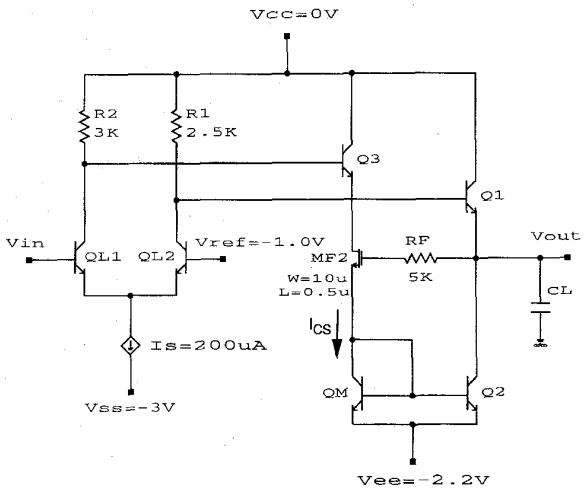


Fig. 7. FCCS-APD-ECL.

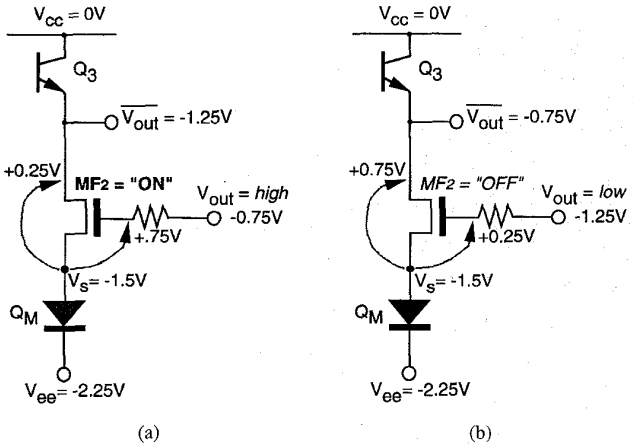


Fig. 8. Voltage on the terminals of the transistor MF_2 in ON (a) and OFF (b) state.

(4) one of the controls for the current path in CCS (2) will be enabled. This, however, will not result in the current in Q_2 because the signal from the logic stage (1) will keep CCS disabled.

During a *High* to *low* transition, the signal from the logic stage enables the current path in CCS (2). Given that the CCS is also enabled (by the output being *high*) the transistor Q_2 will be driven resulting in a fast transition from *high* to *low* at the output. After this transition the output value *low* will be passed with the same delay in the feedback stage (4) to the CCS (2). The CCS will be disabled, reducing the current driving Q_2. This sets the stage for a fast *low* to *high* transition because the output transistor Q_1 does not have to supply excess current to compensate for the current sunk by Q_2. The delay introduced by the feedback stage (4) is necessary to allow sufficient driving current during the *high* to *low* transition as well as to keep Q_2 off during *low* to *high* transition. This delay T_d is set to the maximal tolerable value of the signal edges, $T_d = \max(t_r, t_f)$.

The proposed circuit achieves full push-pull operation while being capable of maintaining reduced voltage swing (of 500 mV in our case). This is achieved by always keeping both transistors Q_1 and Q_2 slightly ON, thus the value of the resistor R_1 can adjust the ouput voltage swing.

III. Implementation

Adhering to the operation described in Section II. this gate can be realized in two ways, one being a purely bipolar realization. A BiCMOS implementation of FCCS-APD-ECL is shown in Fig. 7. This circuit uses a simple RC constant to achieve delay in (4). Feedback delay is achieved by a simple RC network consisting of a resistor R_F and a gate capacitance C_g of transistor MF_2.

The function of the transistor MF_2 is crucial to the operation of this circuit. The gate of MF_2 is connected to the output of the circuit and is driven by a full logic swing, therefore $V_g = [-0.75\text{ V}, -1.25\text{ V}]$. The drain of MF_2 is connected to the transistor Q_2 and it is driven by the exactly same voltages, but in the opposite phase $V_D = [-1.25\text{ V}, -0.75\text{ V}]$. The source of the transistor MF2 is at the constant potential $V_S = -1.5$ V, which is one diode drop above the V_{EE} ($V_{\text{EE}} = -2.25$ V). Relative to the source, the voltage at the MF_2 terminals is shown in Fig. 8 (a) and (b).

The parameters of the transistor MF_2 are: $V_T = 0.4$ V and $L = 0.5\mu$ and $W = 10\mu$ which is achievable in a submicron technology. When the output is *high* the CCS is set for the *high*-to-*low* transition. When the output is *low* CCS is disabled and Q_2 is OFF enabling the true push-pull *low*-to-*high* transition of the output. A delay introduced by the feedback (4) consisting of R_F and C_g is necessary to assure a full transition from *high*-to-*low* before turning MF_2 and Q_2 OFF. This delay is adjusted to be equal to the worse case t_f time and it is not critical in the circuit operation.

The CCS (Fig. 7.) contains a "current mirror" consisting of transistors Q_M and Q_2. The current I_{cs} in the branch consisting of Q_3, MF_2 and Q_M, is "*mirrored*" into the "*pull-down*" output transistor Q_2. The maximal value of I_{cs} is limited by the maximal current transistors Q_3 and MF_2 can provide, which is determined by R_2 and β_{Q_3} as well as the channel resistance of MF_2, (RON). The maximal current in Q_2 is set by the ratio of the emitter areas of Q_2 and Q_M (mirror current). Though, I_{cs} is sensitive to the variations in V_{EE}, those variations are compensated due to the existence of a "negative feedback" from the output to the gate of MF_2. Any increase in I_{cs} (due to the variation of V_{EE}) is thus "reflected" in Q_2, thus lowering V_{out} and reducing I_{cs} (via R_F, MF_2 feedback). The value of V_{EE} is set to three "*diode drops*" ($V_D = 0.75$ V) and therefore it should not be difficult to keep relatively stable.

A bipolar realization of FCCS-APD-ECL is shown in Fig. 9. This allows using a simple bipolar process rather than BiCMOS. However, this version has slightly inferior speed compared to the BiCMOS realization because the voltage swing in the logic stage (1) needed to drive the transistor Q_F to its cut off is larger, therefore degrading the speed of the logic part. Nevertheless, the difference is not considerable.

The output voltage levels across the transistor Q_F are determined by the voltage drop across R_1. The supply voltage

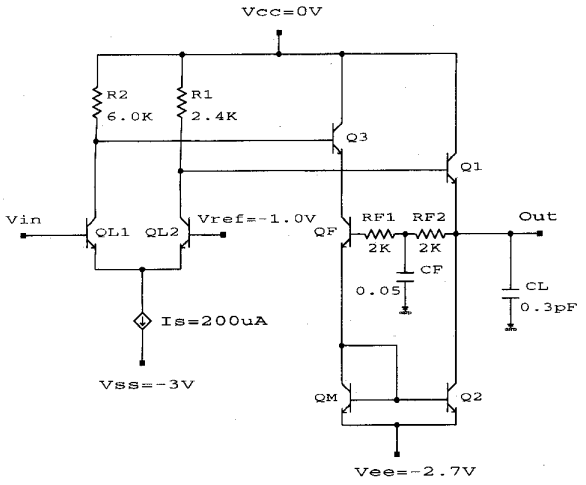


Fig. 9. Bipolar FCCS-APD-ECL.

TABLE I
TYPICAL TRANSISTOR PARAMETERS USED FOR SIMULATION

hfe	100
Tf	6.0pS
Cje	7.54fF
Cjc	3.8fF
Cjs	6.52fF
Re	17.5 ohm
Rb	164 ohm
f_T	20GHz

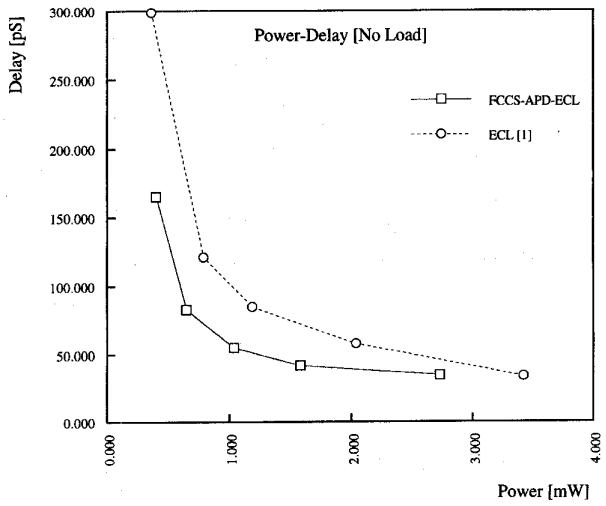
V_{EE} is carefully set to be $V_{EE} = -2.7$ V. This brings the voltage at the emitter of Q_F to be $V_{Fe} = -1.95$ V. The voltage swing across R_1 is 1.2 V, making V_c of Q_F to be $V_c = -1.95$ V enough to turn Q_F off by driving its V_{ce} to zero.

IV. RESULTS AND COMPARISON

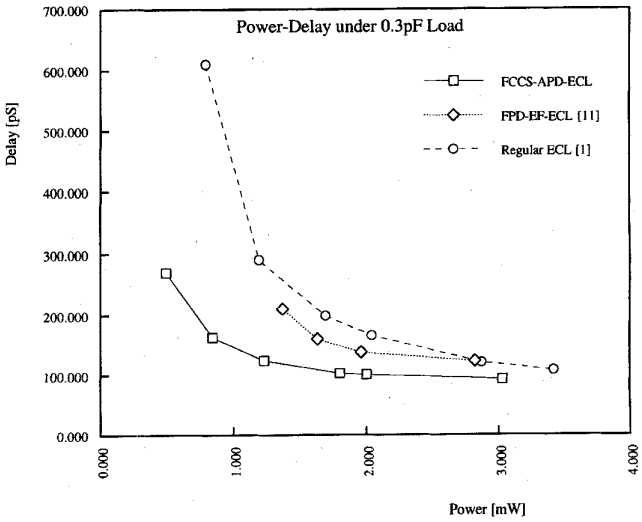
The performance of FCCS-APD-ECL circuit is assessed by simulation using transistor models based on a sub-micron process. For comparison purposes, the simulation parameters shown in Table I and published in [10] were used. The sub-micron transistor models used for simulation in [9]–[11] were not available. Therefore those circuits were re-simulated with our models in order to perform a relative comparison. The relative difference between our circuit and the circuits presented in [9]–[11] should be preserved, though the results are not an accurate representation of the real speed of those circuits.

FCCS-APD-ECL operates faster than the ones reported [7]–[10]. The power-delay product for FCCS-APD-ECL under no-load conditions is shown in Fig. 10(a) and under 0.3 pF load in Fig. 10(b).

FCCS-APD-ECL gate has also better driving capabilities as shown in Fig. 10(b). At 2 mW per gate and at an output load of 0.3 pF, the delay of the FCCS-APD-ECL is 101 pS versus 148 pS of FPD-EF-ECL, 153 pS of AC-CS-APD-ECL, and 166



(a)



(b)

Fig. 10. Comparative power-delay characteristics: FCCS-APD-ECL, FPD-EF-ECL [11], regular ECL (a) Power-delay characteristic: 0.0 pF Load and (b) power-delay characteristic: 0.3 pF load.

pS of regular ECL as used in [1]. Comparison with AC-CS-APD-ECL (of IBM) was difficult because this circuit requires extensive tuning. However our circuit compares favorably for all of the simulated points, as shown in Fig. 10.

All the delay measurements reported are the $T_{\text{delay}} = \max[t_{\text{rise}}, t_{\text{fall}}]$. This is different from a more universal definition of $T_{\text{delay}} = \text{Average}[t_{\text{rise}}, t_{\text{fall}}]$. The reason for the new definition is that the t_{rise} and t_{fall} times in a regular ECL circuit are asymmetric with the delay dominated by $t_{\text{fall}} > t_{\text{rise}}$ The critical improvement is really in the t_{fall} time and we have chosen to emphasize this improvement by taking the worse delay, rather than diminish its effect by taking an average value.

Power consumption of the new gate is lower as compared to previously reported ones. The difference in power for the same delay can be observed in Figs. 10(a) and (b). For example, a

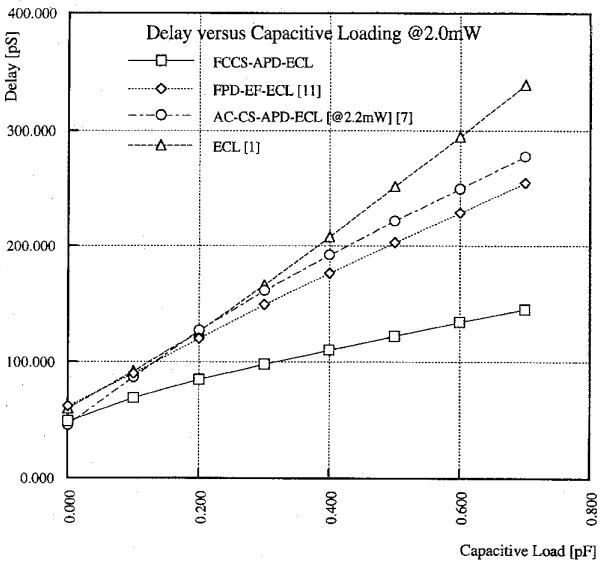


Fig. 11. Delay versus capacitive loading: ECL [1], AC-CS-APD-ECL [10], FPD-EF-ECL [11], FCCS-APD-ECL.

TABLE II
DRIVING CAPABILITY AT 2.0 mW PER GATE

FCCS-APD-ECL	133pS/pF
FPD-EF-ECL [8]	276pS/pF
AC-CS-APD-ECL [7]	328pS/pF
ECL [1]	403pS/pF

200 pS speed for 0.3 pF load is achieved with 0.7 mW of power versus 1.42 mW of FPD-EF-ECL and 1.7 mW for regular ECL. It is also significant to note that the power consumption of the new gate comes for the most part from its logic stage. The output stage has order of magnitude lower power consumption due to its complementary nature.

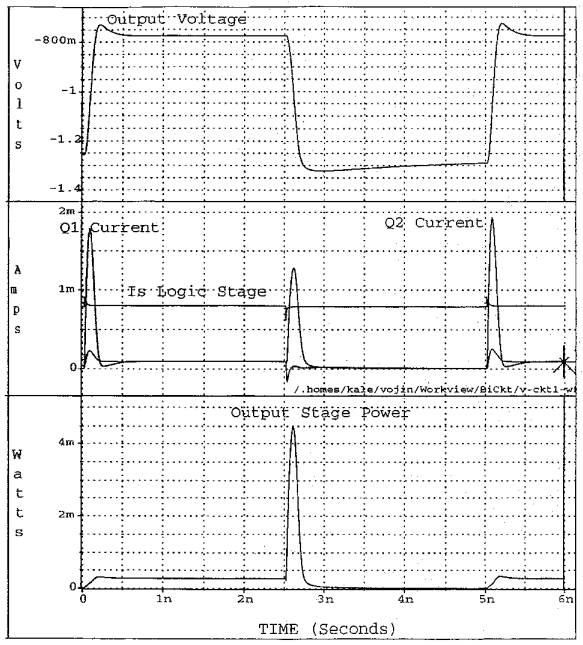
The sensitivity to capacitive load exhibited by the FCCS-APD-ECL gate as compared to [1], [10], and [11] is shown in Fig. 11.

The superior load driving capability of FCCS-APD-ECL is visible from Fig. 11, and the specific data is shown in Table II for the 2.0 mW per gate power.

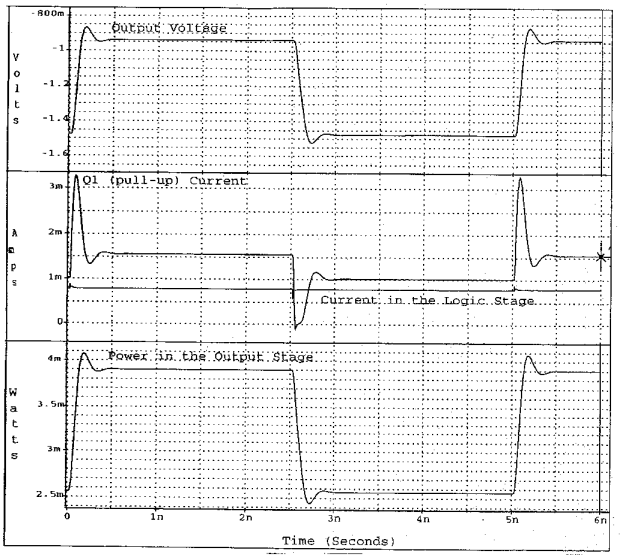
The advantage of the new circuit is especially visible from the output current wave forms. Typical simulated voltage, current, and output power wave forms for our circuit (a), compared to regular ECL [1] (b), are shown in Fig. 12. During the steady state intervals the current in FCCS-APD-ECL circuit is very small. During the transitions this circuit exhibit large current peaks which are responsible for its excellent driving ability. The power generated in the output stages is also shown. When averaged over the signal period the power consumption is small which explains its CMOS-like power behavior.

V. CONCLUSION

The new ECL circuit (FCCS-APD-ECL) shows power advantage over the ones previously reported [7]–[11], yet maintains its speed. This is achieved through a combination of controlled current sources and careful tuning of signal levels and their timing relationships, resulting in increased dynamic and reduced static current in the output stage. Therefore, the major part of the power budget is consumed in the logic stage rather than the output stage, which sets this circuit apart from those previously developed. The ability of this circuit to handle higher capacitive loads is particularly important and offsets its inability for *wired-OR*. This is the main disadvantage



(a)



(b)

Fig. 12. Simulated output voltage, current and power response for the square pulse at the input, for FCCS-APD-ECL versus ECL [1] using 0.3 pF load (a) FCCS-APD-ECL (93 pS delay @ 3.0 mW per gate) and (b) ECL [1] (93 pS delay @5.6 mW per gate).

of this gate compared to FPD-EF-ECL gate [11], which has a remarkably simple structure. The power consumed in the logic part is common to all ECL circuits. Developing circuit techniques which will reduce the power in the logic part is an important and promising area for future work.

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