INTEGRATED POWER CLOCK GENERATORS FOR LOW ENERGY LOGIC

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Abstract – **Low-energy (adiabatic) logic families have been proposed to reduce energy consumption of VLSI logic devices. Instead of the conventional dc power supply, these logic families require ac power supplies (power clocks) that allow energy recovery and also serve as timing clocks for the logic. In this paper, high-frequency resonant dc/ac inverters are proposed as power clock generators where all power switches and control circuitry are integrated on the same chip with low-energy logic. This results in better system efficiency and simpler power distribution. Closed-form results are derived to facilitate efficiency-optimized design of the proposed power clock generators. To illustrate system integration and energy savings, the optimized power clock is used to supply a novel clocked CMOS adiabatic logic (CAL).**

1 Introduction

Motivation to reduce energy consumption of logic circuits comes from increasing difficulties in removing heat from high-speed VLSI circuits, increasingly important and widespread energy-limited, battery-operated applications, and the need to keep the total computer energy usage under control (currently at about $5 - 10\%$ of the total in the USA).

Among techniques proposed to reduce energy consumption, various low-energy (also called *recovered-energy* or *adiabatic*) logic families have recently received much attention [1]-[7]. In the conventional CMOS logic, CV^2 losses are caused by abrupt charging and discharging of internal node capacitances. One may observe that the same mechanism is responsible for a significant part of switching losses in high-frequency switch-mode power converters. In the power conversion area, resonant, zero-voltage and zero-current switching techniques have been used to reduce the switching losses. It is therefore natural that practical low-energy logic implementations can be based on the same techniques applied in resonant power converters.

Instead of dc power, all types of low-energy logic families require ac supply voltages that allow energy recovery and also serve as timing clocks for the logic. The term *power clock generator* is used in this paper to describe the high-frequency resonant dc/ac power converter used to supply the logic. Clearly, efficient power clock generators are needed to realize potential advantages of adiabatic logic in practice. Although some possible power-clock configurations have been indicated [3, 4, 7], most attention in the earlier works has been given to logic operation and performance.

Power clock design based on a self-oscillating dc/ac inverter with external discrete power devices, supplied from a high-voltage dc source, was discussed in more detail in [3]. In a high-power system, ac power distribution problems and packaging issues are of prime concern. In contrast, we consider the application of low-energy logic in compact, low-power, battery-operated systems where energy efficiency is one of the main performance parameters, and a low-voltage dc power source (battery) is available. In this context, integration of power clock generators on the same chip with logic has a number of advantages, as discussed further in this paper.

The paper is organized as follows: operating principles of low-energy logic are briefly reviewed in Section 2. Power-clock requirements are examined for a representative CMOS adiabatic logic proposed in [6]. This is a logic family that requires four phase-shifted power clock waveforms. Next, a novel clocked CMOS adiabatic logic (CAL) that operates with a single power clock is introduced. This logic is used to test operation of a simple power clock generator. Logic model and estimation of model parameters needed for power clock design are discussed in Section 3. Several zero-voltage switching power clock configurations suitable for integration with logic are described in Section 4. In Section 5, we present closed-form results that facilitate efficiency-optimized design of the power clock generators. Section 6 shows how the simple power clock is integrated with the clocked adiabatic logic, together with simulation results that confirm the system operation and the potential for energy savings.

2 Low-Energy, Adiabatic Logic Families

Common to all low-energy (adiabatic) logic families is the periodic exchange of energy between the power clock generator and the logic. The path for energy transfers depends on the logic states. Logic evaluation follows one of several possible

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schemes including *retractile cascade*, *regenerative*, or *memory* schemes [6]. Although logic with asymptotically zero energy loss is feasible [2], memory schemes with partial energy recovery [3]-[7] are preferred because of much simpler and area-efficient implementation.

In memory schemes, each logic stage also performs a memory function so that logic outputs can remain valid even without valid logic inputs. Assuming standard CMOS implementation, an energy loss in the order of $C|V_t|^2$, where $|V_t|$ is the device threshold voltage, accompanies each logic transition when the memory is erased [1]. At present voltage levels, $V_{DD} = 3V$, $|V_t| < 1V$, this is still about an order of magnitude lower loss than CV_{DD}^2 in conventional CMOS logic. Memory schemes, an example of which is given in the next section, offer inherent pipelining, but usually require multi-phase power clocks.

2.1 An Adiabatic Logic Example

Fig. 1 shows a representative CMOS adiabatic logic inverter example [6]. The inverter stage has complementary logic inputs, $F0$ and $\overline{F0}$, and complementary logic outputs $F1$ and $\overline{F1}$. The stage consists of a flip-flop ($M1$-$M4$) and the devices $M5$, $M6$ that implement the logic function. Arbitrary multi-input logic functions can be obtained by replacing the circled devices $M5$, $M6$, with appropriate NMOS logic trees [10] (pp. 311-313). The cross-coupled $M1$-$M4$ provide the memory function, as described in [7].

The stage is supplied by the power-clock PCK shown in Fig. 1 as an idealized trapezoidal waveform. During the *evaluate* interval (A), inputs $F0$ and $\overline{F0}$ must retain their valid logic levels. In the example of Fig. 1, as PCK ramps up, the output $F1$ stays at zero, while energy is delivered from the power clock to the node capacitance at the complementary $\overline{F1}$ output. During the *hold* interval B, the outputs $F1$ and $\overline{F1}$ remain valid, while the inputs may change toward zero. In the *precharge* interval (C), the output $\overline{F1}$ is discharged from V_{DD} toward zero, partially returning energy from the node capacitance to the power-clock generator. $M2$ in the discharge path turns off when PCK falls below the device threshold voltage $|V_t|$. Therefore, a part of the energy remains stored on the node capacitance at the $\overline{F1}$ output. In the *idle* interval (D), the inputs may assume new valid values. A change in the logic input causes a loss of the residual energy at the $\overline{F1}$ output, through $M6$. Just as in resonant power converters, any additional energy losses are due to non-zero forward voltage drops of elements in the conducting path, but these losses can be reduced arbitrarily by reducing the current magnitudes (for example by decreasing the clock frequency) or by reducing the device on-resistances.

In a cascade connection of the logic stages, it is necessary to ensure that the *hold* interval of one stage coincides with the *evaluate* interval of the next stage. Therefore, *four* phase-shifted power clock waveforms are needed for proper stage-to-stage interface. The system timing for a chain of logic stages is shown in Fig. 2. The four power clock waveforms PCK, PCK1, $\overline{\text{PCK}}$ and $\overline{\text{PCK1}}$ are phase-shifted by one-fourth of the clock period.

Several other adiabatic low-energy logic families have been

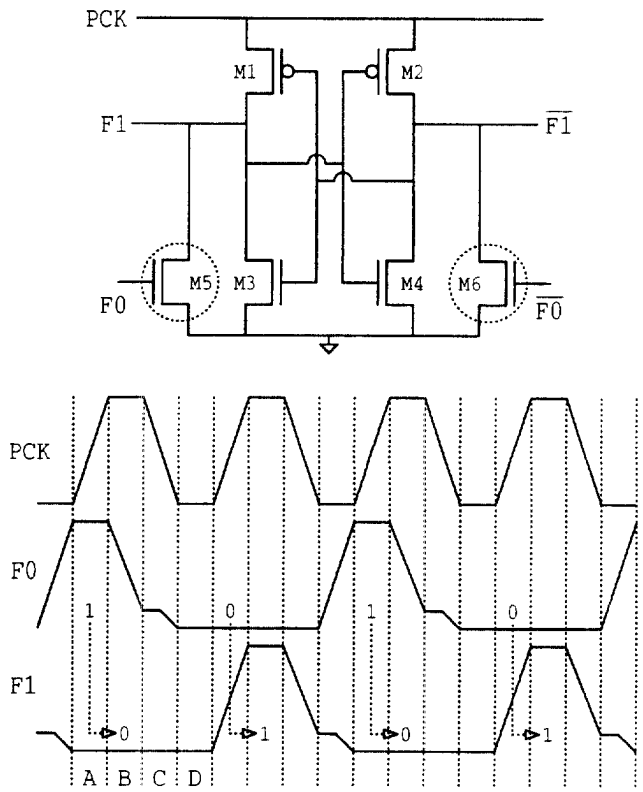

Figure 1: Inverter in the logic family of reference [6].

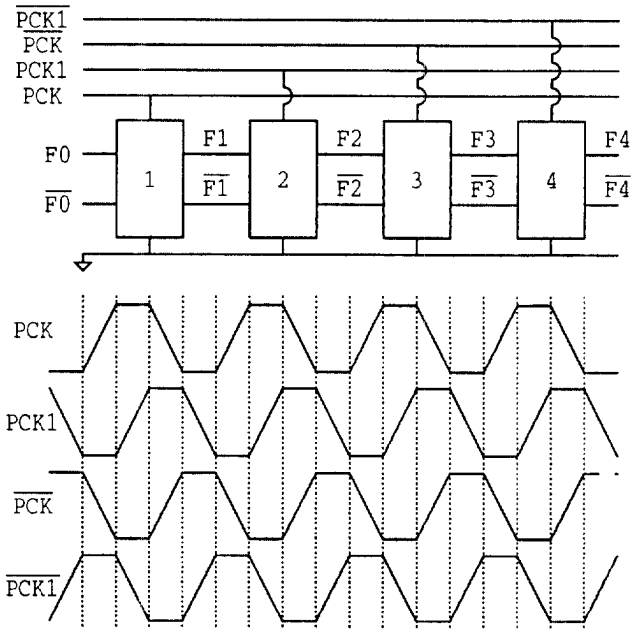

Figure 2: System waveforms in the adiabatic logic family of Fig. 1: four phase-shifted power clocks are needed.

proposed with similar power clock requirements [4, 5, 7]. The problem of efficiently generating and distributing the multi-phase power clocks clearly becomes a limiting factor for these low-energy logic schemes.

An exception among memory schemes is the *recovered-energy logic* (REL) [3], where only one power clock is required. This was achieved by implementing logic stages alternatively with n or p devices, and by overlapping the precharge and the evaluate intervals. However, disadvantages of REL include bipolar implementation, increased additional conduction losses due to V_{BE} or V_{CES} voltage drops, ability to implement only simple logic functions per stage, and relatively low noise margins.

2.2 Clocked Adiabatic Logic with a Single Power Clock

In this section we introduce an adiabatic logic that operates with a single power clock, has simple CMOS implementation, and good noise immunity.

The basic inverter stage of the *clocked low-energy logic* (CAL) is shown in Fig. 3. The CAL stage topology is a modification of the adiabatic logic shown in Fig. 1, with the clocked *enable* devices $M7$, $M8$ added in series with the logic trees. The purpose of the modification is to allow operation with a single power clock PCK. The CAL timing differs significantly from the logic in Figs. 1 and 2.

Idealized CAL timing waveforms are shown in Fig. 3. In the clock period A, the auxiliary clock CX enables the logic evaluation. For $F0 = 0$, $M8$ and $M6$ are on, $\overline{F1} = 0$, $M1$ is on, and the output $F1$ closely follows the power clock waveform. In the next clock period B, the auxiliary clock CX = 0 disables the logic evaluation. The previously stored logic state is repeated at the outputs $F1$ and $\overline{F1}$, regardless of the inputs, so that the stage that follows can perform logic evaluation.

System waveforms are shown in Fig. 4. All logic stages are supplied by the same power clock PCK. The logic evaluation is enabled in alternate logic stages by the auxiliary clock CX and its complement $\overline{CX}$. Because of the memory function, pipelining is inherent, as in other memory adiabatic schemes. The auxiliary clocks drive *only* device gates so that the additional energy loss can be minimized by reducing the clock amplitudes, or by using a high-efficiency resonant clock scheme. The overhead loss is relatively small, especially when more complex logic functions are implemented in CAL stages. Since the logic operates with a single power clock, a very simple, power and area efficient power-clock generator can be applied. The low-power auxiliary clocks can be distributed using the same techniques used in conventional clocked CMOS. Therefore, power and clock distribution are simpler and more efficient than in multi-phase adiabatic logic families.

3 Low-Energy Logic Model

Low-energy logic presents a capacitive load to the power clock generator. For each phase, an approximate lumped-element model of the logic includes an equivalent capacitor C to model the energy storage, in series with a resistor R to model the losses. By complementing the logic function in each logic

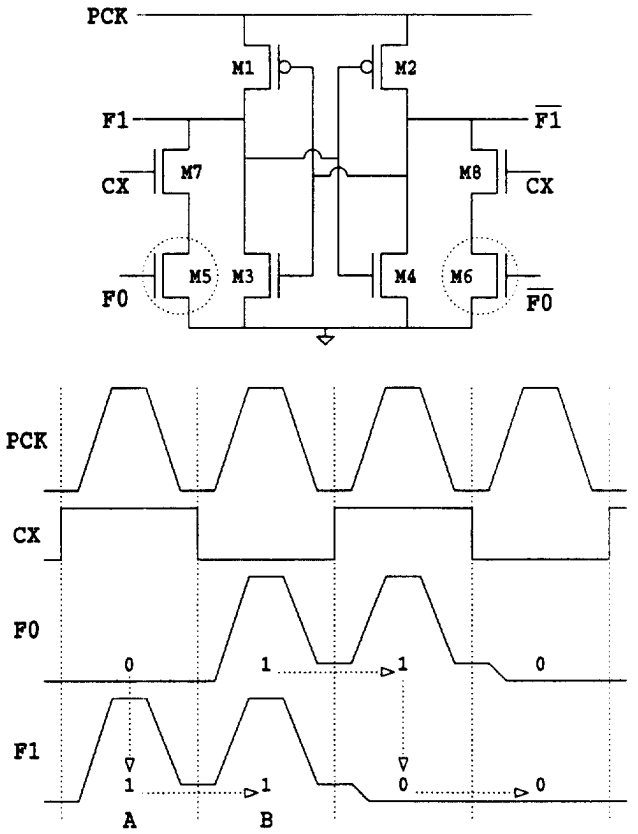

Figure 3: Inverter in the clocked adiabatic logic (CAL).

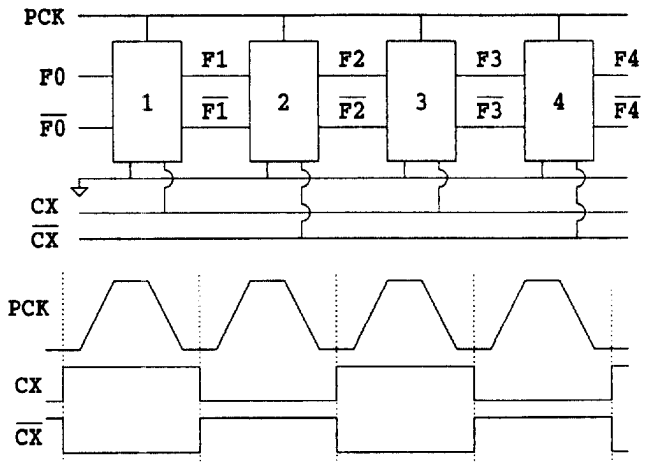

Figure 4: System waveforms in the clocked adiabatic logic.

stage, as in the logic families of Fig. 1 or Fig. 3, the equivalent capacitive load C becomes approximately independent of the logic states or the logic activity. This simplifies the power clock design based on resonant power conversion techniques. It is important to note that changes in the logic activity correspond to loss variations and so the equivalent resistance R depends on the logic activity.

Logic model parameter values R and C can be extracted from simulation tests (or experiments) where external ideal sinusoidal voltage sources are applied as power clocks. For a given clock frequency f_c, and logic activity, the objective of the test is to determine the power loss P_L in the logic, and the rms current I_L supplied to the logic by the power clock. For power-clock design purposes, the tests should be performed for the logic activity that corresponds to the worst-case losses. Given P_L and I_L, the model parameters can be found as:

$$R = \frac{P_L}{I_L^2}, \tag{1}$$

$$C = \frac{\sqrt{2} I_L}{\pi V_{DD} f_c}. \tag{2}$$

As an indication of the logic power loss P_L relative to the maximum loss $CV_{DD}f_c$ that would occur in the plain CMOS logic with the same C, we find

$$y_L = \frac{P_L}{CV_{DD}^2 f_c} = \frac{\pi}{\sqrt{2}} \frac{P_L}{V_{DD} I_L} = \frac{\pi^2}{2} RCf_c. \tag{3}$$

The simulation test has been performed at $V_{DD} = 3$V with a chain of 10 CAL inverters using a 0.8μ CMOS technology, for a range of clock frequencies, and the results are summarized in Table 1. The tests are performed for the maximum logic activity corresponding to the periodic logic states $\cdots 0101 \cdots$ propagating through the chain of inverters.

f_c[MHz]	$P_L[\mu W]$	$I_L[\mu A]$	$R[\Omega]$	y_L[%]
10	2.6	23	4805	8.4
20	6.1	46	2835	9.7
30	10.5	69	2200	11.1
40	16.4	92	1926	13.0
50	24.5	117	1790	15.6
60	31.0	139	1605	16.4
70	40.5	162	1535	18.3
80	51.4	186	1490	20.4
100	80.6	234	1466	25.6

Table 1: Results of simulation tests for $V_{DD} = 3$V on a chain of 10 CAL inverters supplied with an ideal sinusoidal power clock, and with the logic input $\cdots 01 \cdots$. The equivalent capacitive load $C = 350$fF is independent of the clock frequency f_c.

4 Integrated Power Clock Generators

Our approach to power clock design is to integrate all power-clock switching transistors and associated control circuitry on the same CMOS chip with low-energy logic. Only small resonant-tank inductor(s) are added as external components. The power is supplied from a low-voltage dc power source, a battery for example. Integration of power clock generators with logic has a number of advantages:

(a) the on-chip active devices are well suited for low-power, low-voltage power conversion, and the device sizes are available for optimization at design time;

(b) power-clock distribution is improved because relatively large and detrimental parasitic inductances are removed from the distribution network; bonding-wire and other external parasitic inductances are absorbed by the external resonant-tank inductor(s);

(c) external discrete component count is minimized;

(d) on-chip power-clock control circuitry can easily be implemented: sensing of power-clock waveforms for control purposes is void of delays/noise introduced by the chip i/o interface.

Common to the proposed power clock generators are the following characteristics:

(a) An external inductor and the equivalent logic capacitance form a resonant tank. Power clock generator operates as high-frequency, resonant, unloaded dc/ac inverter.

(b) In order to minimize conduction losses, no active devices in the power clock are placed in series with the inductor or in series with the logic.

(c) All active devices in the power clock are soft-switched at zero voltage in order to minimize switching losses.

(d) Active control of the switching devices allows control over the power-clock waveforms, simple synchronization, and simple generation of multiple phase-shifted waveforms.

4.1 1N Single-Phase Power Clock Generator

The simplest power-clock generator considered here is the 1N single-phase generator of Fig. 5. The generator consists of a single NMOS active device Q (hence "1N") in parallel with logic, and a single resonant-tank inductor L_r in series with the dc source $V_{DD}/2$.

Transistor Q is turned on for a brief interval $t_{on} = D/f_c$ in each clock period, only to add energy lost in the L_rC resonant tank. The turn-on is at zero voltage. The switch duty ratio D can be controlled to regulate the power clock amplitude (which is ideally equal to V_{DD}) if the available dc voltage is not well regulated, or to compensate for load variations caused by changes in logic activity.

Fig. 6 shows typical waveforms in the 1N power clock generator. The results are obtained for $f_c = 10$MHz, and for the RC load as shown in Fig. 5. The parameters are as in the first row of Table 1. The dc supply voltage is $V_{DD}/2 = 1.5$V.

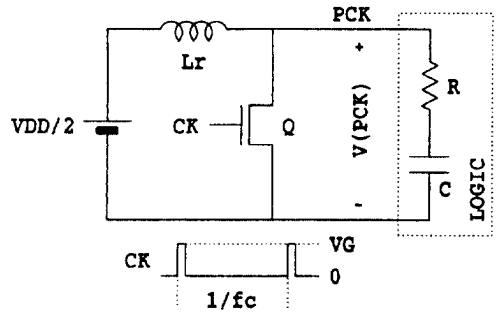

Figure 5: 1N Single-Phase Power Clock Generator.

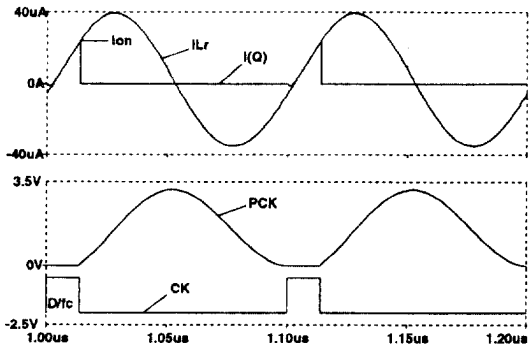

Figure 6: Typical steady-state waveforms in the 1N power clock generator of Fig. 5 at $V_{DD}/2 = 1.5$V, $f_c = 10$MHz.

4.2 1N1P Single-Phase Power Clock Generator

A two-transistor version of the single-phase power clock generator is the 1N1P power clock generator shown in Fig. 7, together with gate-drive signals for the two switches. The PCK amplitude is clamped to V_{DD}. The PMOS is turned on by the gate drive CK1 at zero voltage, at the peak of the power-clock waveform PCK across the logic. Similarly, the NMOS is turned on by the gate drive CK2 at zero voltage, at the valley of PCK. The large energy-storage capacitor C_s stays charged at approximately $V_{DD}/2$ dc voltage.

In [8] this power clock has been described in detail as an ideally lossless gate-drive circuit for MOS power devices. Here, the load is low-energy logic, but the operating principles are the same. By adjusting the device on/off timing, and the device duty ratios, it is possible to obtain a near-trapezoidal power-clock waveform PCK, which may result in better noise margins and lower losses in the logic. The results from [8] and [9] can be applied in this case.

4.3 2N2P Two-Phase Power Clock Generator

A simple extension of the 1N1P power clock is the 2N2P power clock generator in Fig. 8. It generates two complementary power clock waveforms using only one inductor.

The gate-drive waveforms shown in Fig. 7 correspond to the fully controlled switch-mode version where all four devices are switched on and off by the gate-drive signals CK1-CK4.

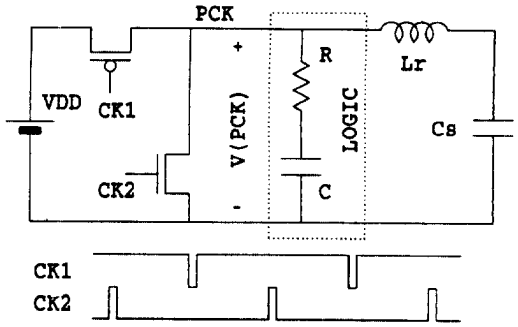

Figure 7: 1N1P power clock generator.

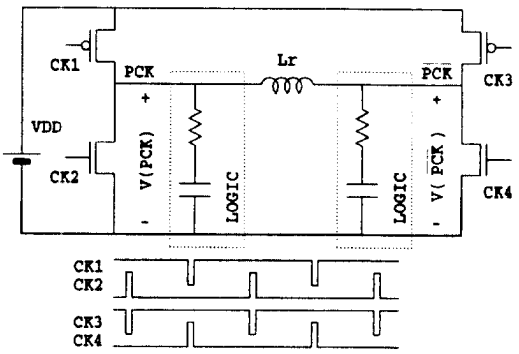

Figure 8: 2N2P two-phase power clock generator.

A self-oscillating scheme can be obtained by cross-coupling $CK1 = CK2 = \overline{PCK}$, $CK3 = CK4 = PCK$ [4]. The scheme has an advantage of eliminating the gate-drive losses and control circuitry, but at the expense of more difficult synchronization, loss of control, and lower efficiency because of higher conduction losses.

A half-controlled version that combines some of the benefits of the fully-controlled and the self-oscillating versions has $CK1 = \overline{PCK}$ and $CK3 = PCK$, while the NMOS devices are controlled by the gate-drive signals $CK2$ and $CK4$.

5 Power Clock Design

We first examine properties of logic CMOS devices when used as power switches. Then, closed-form results are derived for efficiency-optimized design of power clock generators.

5.1 Logic CMOS devices as power switches

NMOS and PMOS devices in a standard CMOS technology are well suited for on-chip power conversion at low voltage and low power levels. This has recently been demonstrated in a CMOS dc-dc converter [11].

Using the first-order device model [10] (pp. 51-53), the device on-resistance with $V_{ds} \approx 0$ is given by

$$R_{on} = \frac{1}{K_p \frac{W}{L}(V_G - V_t)}, \qquad (4)$$

where V_t is the threshold voltage, W and L are the effective

channel width and length, $K_p = \mu_n C_{ox}$ is the device transconductance parameter, μ_n is the electron mobility (for NMOS devices), and C_{ox} is the gate-to-channel capacitance per unit area. The device input (gate) capacitance at $V_{ds} \approx 0$ is:

$$C_g = WLC_{ox} . \tag{5}$$

The product $C_g R_{on}$ determines the high-frequency power-handling capability of the device. For the considered 0.8μ CMOS technology, with $V_G = 3\text{V}$, $V_t = 0.7V$, $K_p = 120\mu A/V^2$, and $C_{ox} = 1.42fF/\mu^2$, we have

$$C_g R_{on} = \frac{L^2}{\mu_n (V_G - V_t)} \approx 5ps , \tag{6}$$

which is significantly lower than in currently available discrete power devices.

Consider a device switched at zero voltage by a square-wave drive with amplitude V_G, and conducting rms current equal to I_s. The total device power loss P consists of the gate-drive switching loss and the device conduction loss:

$$P = mWLC_{ox} V_G^2 f_c + \frac{I_s^2}{K_p \frac{W}{L}(V_G - V_t)} . \tag{7}$$

The standard technique to drive large capacitive loads is with a chain of ratioed CMOS inverters [10] (pp. 229-230). The factor $m > 1$ in the power-loss expression models the additional losses in the ratioed stages. For the usual stage ratio of 3, $m \approx 1.5$. Minimization of the power loss with respect to the device size W and the gate drive amplitude V_G yields the optimum values:

$$(V_G)_{\text{opt}} = 2V_t , \tag{8}$$

$$W_{\text{opt}} = \frac{I_s}{\sqrt{8mK_p C_{ox} V_t^3 f_c}} . \tag{9}$$

The minimum power loss is given by

$$P_{\text{min}} = 4LI_s \sqrt{m \frac{V_t}{\mu_n} f_c} . \tag{10}$$

It is interesting to note that the optimum gate drive amplitude V_G is always $V_G = 2V_t$, regardless of the power level. The device size, and the minimum power loss are proportional to the device rms current I_s. The technology scaling (reducing the minimum channel length L) contributes to lower losses and improved efficiency, as long as the assumptions of the above analysis are valid.

5.2 Optimum Power Clock Design

The power clock design can be optimized for efficiency using the results obtained in Section 5.1. Results are presented here only for the 1N power clock generator shown in Fig. 5, but can easily be extended to other power clock configurations.

To determine the switch Q rms current, we observe that the switch current during the D/f_c interval is increasing from zero approximately as a linear function of time. The relevant waveforms are shown in Fig. 6. During the switch on-time, energy is added from the dc power source $V_{\text{DD}}/2$ to the resonant tank.

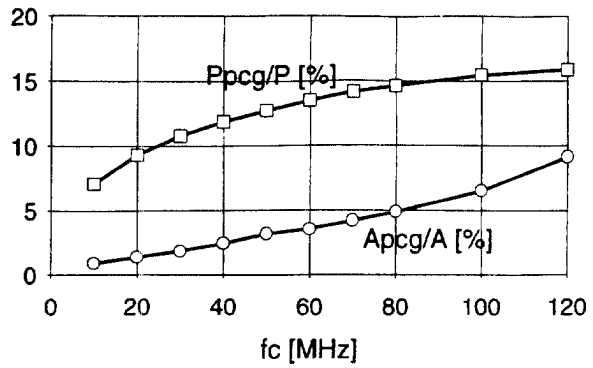

Figure 9: Power loss P_{pcg} and active gate area A_{pcg} relative to the total power loss P and the total area A, as functions of the clock frequency f_c.

When the switch Q is turned off, the energy is dissipated during the oscillation. For a sustained steady-state oscillation, we have the required energy balance given approximately by:

$$\frac{1}{2} L_r i_{on}^2 = \frac{P_L}{f_c} . \tag{11}$$

The clock frequency f_c is approximately equal to the resonant frequency, $f_c \approx 1/2\pi\sqrt{L_r C}$. Combining Eqs. (2), (3), and (11), we solve for the switch current i_{on} at the end of the switch on-time, and for the required switch duty ratio D,

$$i_{on} = 4I_L \sqrt{y_L} . \tag{12}$$

$$D = \frac{\sqrt{2y_L}}{\pi} . \tag{13}$$

The switch rms current I_s is then given by:

$$I_s = i_{on} \sqrt{\frac{D}{3}} = 1.55(y_L)^{0.75} I_L . \tag{14}$$

Once the switch rms current I_s is determined, Eqs. (9) and (10) can be used to determine the optimum device size and the minimum power loss in the power clock generator.

Fig. 9 shows the results obtained when the optimized 1N power clock is used to supply the chain of CAL inverters with the parameters given in Table. 1. The power clock loss P_{pcg} ranges from 7% (at $f_c = 10\text{MHz}$) to 16% (at $f_c = 120\text{MHz}$) of the total loss $P = P_{pcg} + P_L$. The gate area A_{pcg} of the switch Q relative to the total gate area ranges from less than 1% (at $f_c = 10\text{MHz}$) to 9% (at $f_c = 120\text{MHz}$).

6 System Integration and Simulation Results

Simulation tests have been performed on the chain of CAL inverters supplied by the 1N power clock generator, as shown in Fig. 10. The dc source is $(V_{\text{DD}}/2) = 1.5\text{V}$, and the clock frequency is $f_c = 20\text{MHz}$. The auxiliary clocks CX and $\overline{CX}$ are obtained easily from the gate drive signal CK for the switch Q in the power clock generator. Both the gate drive and the auxiliary clocks are 0-to-$V_{\text{DD}}/2$ square waves. The gate-drive amplitude (1.5V) is very close to the optimum ($2V_t$) value.

Fig. 11 shows the waveforms obtained by Spice simulation of the system in Fig. 10. The total energy loss at this clock

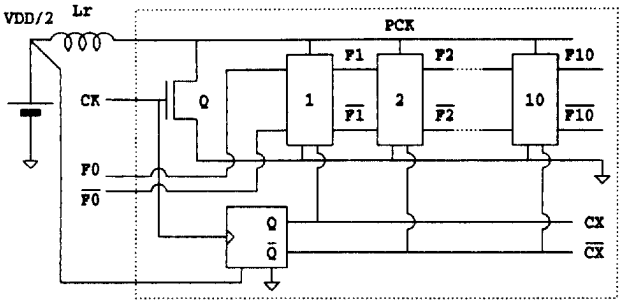

Figure 10: The 1N power clock generator integrated with a chain of CAL inverters.

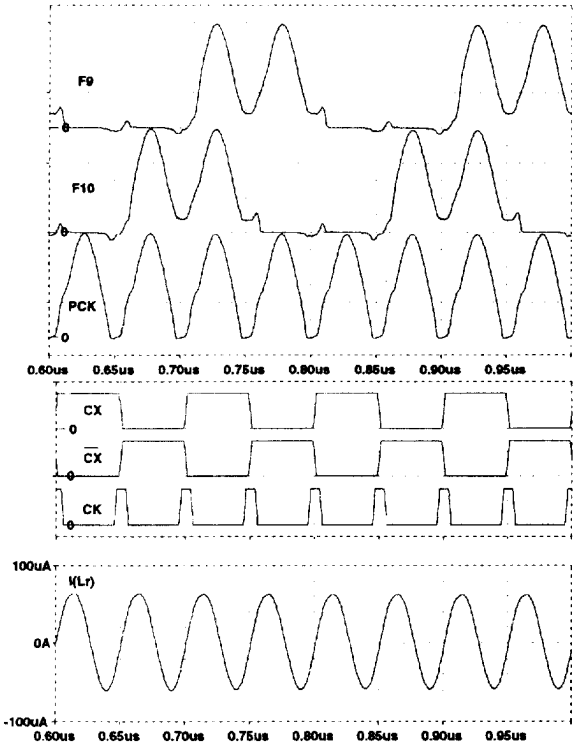

Figure 11: Spice simulation results for the system of Fig. 10 at $V_{DD} = 1.5$V, $f_c = 20$MHz.

frequency is $W = 42$fJ per stage, where 29fJ (69%) is the logic loss, 10fJ (24%) is the loss in auxiliary clocks, and 3fJ (7%) is lost by the power clock generator. The power-clock loss is somewhat lower than the value predicted by the results of Section 5.2.

7 Conclusions

Low-energy, adiabatic CMOS logic has the potential of significantly reducing power consumption of digital VLSI devices. Efficient power-clock generators are necessary to facilitate practical implementation of adiabatic logic. This paper shows how power- and area-efficient power clock generators can be designed on the same chip with logic, and supplied from a low-voltage dc source. The proposed power clock generators are based on zero-voltage switching resonant techniques where a small external inductor forms a resonant circuit with the equivalent logic capacitance. Control of power-clock devices allows active regulation of the power clock waveforms, simple synchronization, and generation of multi-phase waveforms, as required in several adiabatic logic families.

It is shown that the on-chip devices in standard CMOS technology are very well suited for low-power, low-voltage power conversion. Closed-form results are derived for efficiency-optimized design of the power clock generators. For a range of clock frequencies, the power clock generator spends about 10% of the total energy loss, and takes less than 10% of the chip area.

A novel clocked CMOS adiabatic logic (CAL) is described in the paper. It operates with a single power clock waveform that can be generated using a power clock generator with only one active device. Simulation tests on the system consisting of the power clock generator and a chain of CAL inverters indicate significant energy savings and reliable operation.

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