An ECL Gate with Improved Speed and Low Power in BiCMOS Process

Vojin G. Oklobdzija

Advanced Computer Systems Engineering Laboratory
Department of Electrical and Computer Engineering
University of California
Davis, CA 95616
vojin@ece.ucdavis.edu

Abstract - An ECL gate exhibiting an improved speed-power product over the circuits presented in the past [1,3-7] is described. The improvement is due to a combination of a push-pull output stage driven by a controlled current source. This circuit has better driving capabilities and improved speed, yet it uses an order of magnitude less power than regular ECL gate. Fully bipolar realization of this circuit is also possible.

1. INTRODUCTION

ECL [1] has gained new attention in high-performance systems [2] and showed some renewed promise.

There are two inherent advantages of using ECL structures: (a) switching current in a bipolar differential pair is much faster than what can be achieved with MOS transistors. (b) the voltage swing of the signal propagated through the wire is much smaller than in a comparable CMOS structure.

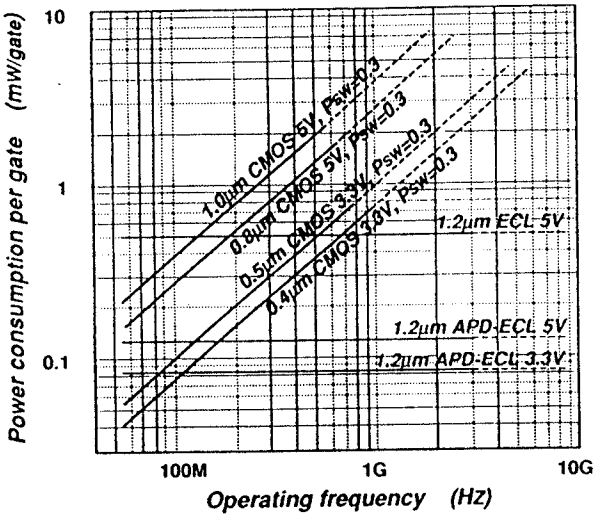


Fig. 1. *ECL-CMOS Speed-Power Trade-off [9]*

The reduced voltage swing helps in reducing the propagation delay as well as power consumption given that the dynamic portion of the power consumed in the chip is given as:

$$P_0 = f_0 \times C_L \times V_S^2$$

At very high frequencies of operation the power consumption of CMOS can be quite substantial and therefore it is common misunderstanding to treat CMOS as a low power technology. This fact is illustrated very well in a chart provided by Kuroda [9] shown in Fig. 1.

A very important part of an ECL gate is its driving stage. This is where most of the power is being used to provide sufficient driving ability. Also the speed of the gate is determined by how much dynamic current can be provided by the output drive stage.

In a regular ECL gate the switching speed is determined by the value of the resistor in the path to V_{ee} [1]. This creates a direct relation between the static and dynamic current. Any increase in the dynamic current results in more power being consumed by the gate.

Authors from IBM have developed several ECL structures using active-pull-down bipolar combination in the output (APD-ECL) [3-5]. A review of those techniques is given in [4]. They have described various structures in which a path is provided from the logic tree of the ECL structure to the "*pull-down*" output transistor resulting in an extra amount of charge being injected into its base when needed to speed-up the transition. Their circuit results in faster operation at lower power, compared to regular ECL. The operation of APD-ECL of IBM [4] is illustrated in Fig.2.

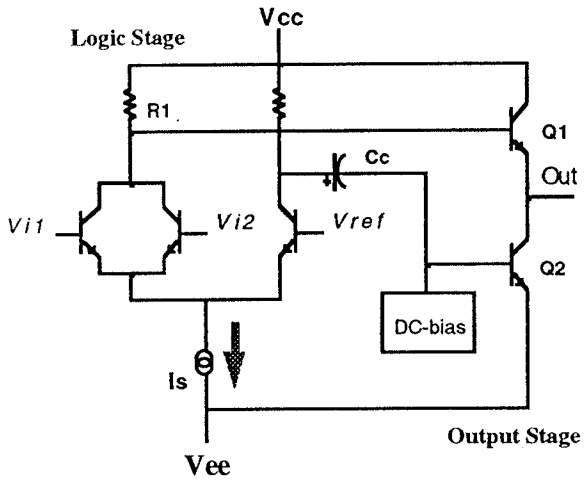


Fig. 2. *APD-ECL from IBM [4]*

Other refinements of the APD-ECL family are AC-APD-ECL [5] and AC-CS-APD-ECL [6], the latter being slightly faster than [5]. Despite its remarkable performance AC-CS-APD-ECL has some shortcomings. The operating point of the output stage in AC-APD-ECL is dependent on the operating point of its logic stage. This dependency makes it difficult to make adjustments in the logic stage, especially if one is to try to reduce power. Also any adjustment of the operating point involves both logic and output stages which makes this process rather difficult. It is also difficult to *cascode* the logic higher than one level. The *emitter-doting* operation is not permitted either.

Recently, several other very effective ECL circuits were reported [7,8] most notably the circuit developed by H.J. Shin of IBM termed FPD-EF-ECL [7]. This circuit has a remarkable simplicity while yielding several benefits such as the ability to permit *emitter doting*. However, those schemes were not able to significantly reduce the *static* current in the output stage, which also affected the driving capability and in turn the speed of the gate.

0-7803-2117-0/94/$4.00 © 1994 IEEE

2. CIRCUIT OPERATION

A new circuit has been developed that utilizes Feedback-Controlled-Current-Source in an Active-Pull-Down ECL configuration (FCCS-APD-ECL) [11]. A controlled current source is used to inject current into the pull-down transistor of its output stage during transition periods. In a steady-state this current is reduced to its minimum value. This circuit has a better power-delay product than ones previously reported [3-6] due to the fact that its output stage is operating in truly push-pull mode of operation. The power consumed in the output stage is an order of magnitude lower than in its counterparts yet maintaining comparable speed. The ability to drive large capacitive loads is substantially improved. There are several benefits resulting from this configuration:

(a) The logic stage is decoupled from the noise which is generally generated in the output stage.

(b) The operating point of the output stage is not dependent on the logic stage, therefore the logic can be cascoded in more than one level, thus allowing for more complex logic operations within one ECL tree. This is not possible in AC-CS-APD-ECL [6].

(c) Reduced power supply voltage in the output stage results in an overall power reduction, given that the output stage is a main contributor to the power budget.

The proposed circuit achieves full push-pull operation yet is capable of maintaining reduced voltage swing (of 500 mV in our case). This is achieved by always keeping both transistors Q_1 and Q_2 slightly ON thus the output voltage swing is adjustable by adjusting the value of the resistor R_1.

Conceptual operation of this circuit is summarized in Fig.3, which illustrates the major parts of this circuit. The circuit consists of an ECL logic tree (1), controlled current source (2), output driver stage (3) (consisting of the transistors Q_1 and Q_2) and feedback stage (4). The current source is controlled by the logic stage as well as the feedback stage.

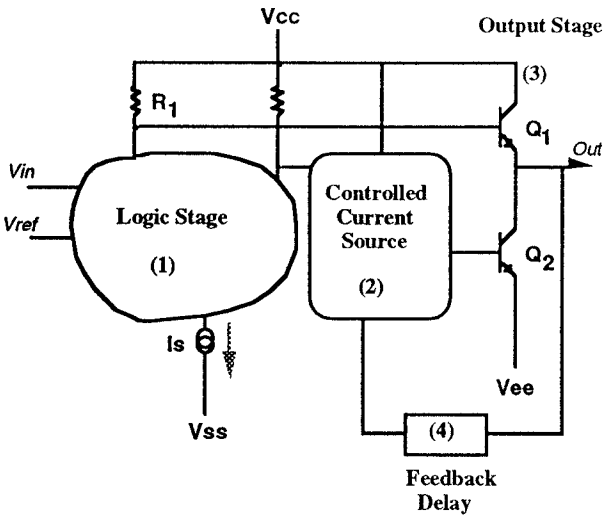


Fig. 3. *FCCS-APD-ECL Circuit Operation*

High current induced by (2) into the output transistor Q_2 assures sufficient current drive for the output transistor Q_2 to rapidly discharge the load capacitance C_L and drive the output node from *high* to *low* state. Output transistor Q_1 is driven directly from the logic stage. The current in the *current mirror* of the current source (2) is controlled by the logic stage (1) and it is in the opposite phase of the current driving the output transistor Q_1. This assures that the transistors Q_1 and Q_2 are driven in opposite phases thus eliminating direct current path from V_{cc} to V_{ee}.

Low to High transition of the output stage is achieved by driving Q_1. The output node will assume *high* value and after a set delay through the feedback path (4) it will enable a current path in the *current mirror* of the controlled current source (2). However, it will not result in *high current* because the input from the logic stage (1) will keep the controlled current source in the *low current* mode.

During *High to Low* transition, the signal from the logic stage enables the current path in the current source (2). The transistor Q_2 will be driven by a *high current* from the *current mirror* thus resulting in a fast transition from *high to low* at the output. After this transition the output value *low* will be passed with same delay in the feedback stage (4) to the controlled current source (2). The path of the *current mirror* will be disconnected, thus reducing the current driving Q_2. This sets the stage for a fast *low to high* transition because the output transistor Q_1 does not need to supply current to compensate for the current sunk by Q_2. The delay introduced by the feedback stage (4) is necessary to allow sufficient driving current during the *high to low* transition.

3. IMPLEMENTATION

Following the principles of the circuit operation described in section 2, the circuit can be realized in several ways, of which purely bipolar realization is also possible. A simplified version of this circuit using a simple RC constant to achieve delay in (4) (RC-FCCS-APD-ECL) [11] is shown in Fig.4. Feedback delay is achieved by a simple RC network consisting of a resistor R_F and a gate capacitance C_g of transistor MF_2.

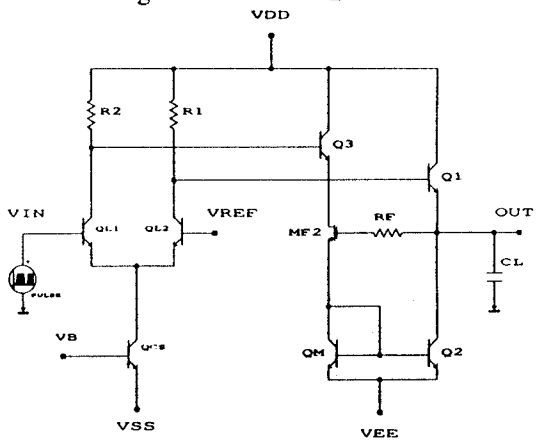
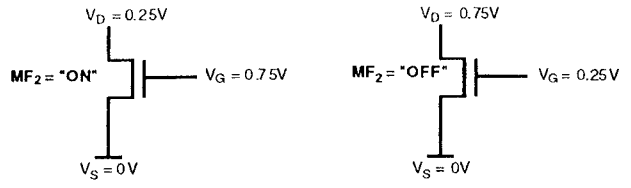


Fig.4. *RC-FCCS-APD-ECL [11]*

The function of the transistor MF_2 is crucial to the operation of this circuit. The gate of MF_2 is connected to the output of the circuit and it is driven by a full logic swing, therefore V_g = [-0.75V, -1.25V]. The drain of MF_2 is connected to the transistor Q_2 and it is driven by the exactly same voltages, but in the opposite phase V_D = [-1.25V, -0.75V]. The source of the transistor MF_2 is at the constant potential V_S = -1.5V, which is one diode drop above the V_{EE} (V_{EE} = -2.2V). Relative to the source, the voltage at the MF_2 terminals is shown in Fig. 5. (a) and (b). The results presented in this paper were obtained by simulation using RC-FCCS-APD-ECL implementation. Therefore in the further text when referring to FCCS-APD-ECL we will assume the RC-FCCS-APD-ECL realization.



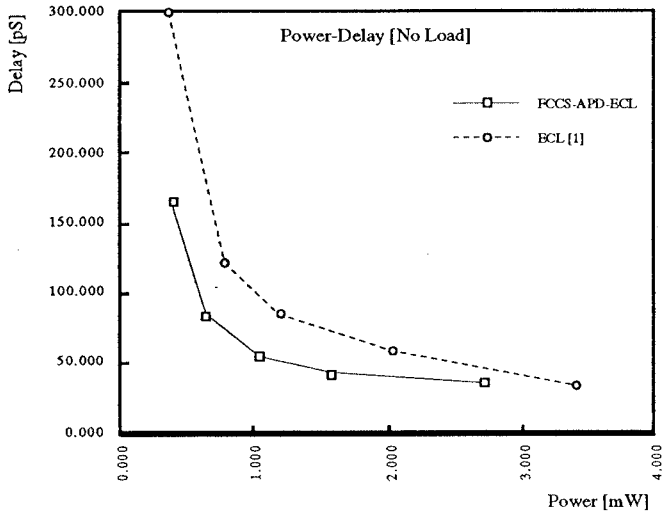
(a) MF_2 in ON state *(b) MF_2 in OFF state*

Fig. 5. *Voltage on the terminals of the transistor MF_2*

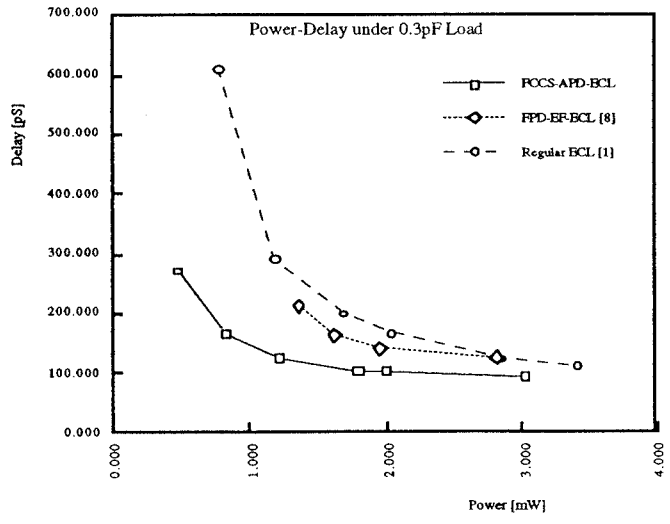
4. RESULTS AND COMPARISON

The performance of our FCCS-APD-ECL circuit is assessed by simulation using transistor models based on sub-micron process. For comparison purpose the simulation parameters published in [6] were used. They were not complete and therefore our parameters are *semi-academic* and are not an accurate representation of the real speed of the circuits presented. However, the relative difference between our circuit and the circuits in presented in [5-7] should be preserved.

The new ECL gate operates faster than the ones reported in [3-6]. The new circuit delay under no-load conditions is shown in Fig. 6 (a) and under 0.3 pF load in Fig. 6 (b).



(a) Power -Delay Characteristic: 0.0 pF Load



(b) Power -Delay Characteristic: 0.3pF Load

Fig.6. *Comparative Power-Delay Characteristics FCCS-APD-ECL, FPD-EF-ECL [7], regular ECL*

The new ECL gate has better driving capabilities shown in Fig. 6 (b). At 2mW per gate and an output load of 0.3 pF, delay of FCCS-APD-ECL is 101pS vs.148pS [8], 153pS [6] and 166pS of regular ECL [1]. Comparison with AC-CS-APD-ECL was difficult because this circuit requires an extensive tuning. However our circuit compares favorably for all of the simulated points taken as shown in Fig. 7.

Power consumption of the new gate is lower than that of the previously reported ones. The difference in power for the same delay can be observed in Figs. 6 (a) and (b). For example, a 200 pS speed for 0.3pF load is achieved with 0.7 mW of power versus 1.42 mW [8] and 1.7 mW for regular ECL. It is also significant to note that the power consumption of the new gate comes for the most part from its logic stage. The output stage has order of magnitude lower power consumption due to its complementary nature.

All the delay measurements reported are the $T_{delay} = \max[t_{rise}, t_{fall}]$. This is different from a more universal definition of T_{delay} = Average $[t_{rise}, t_{fall}]$. The reason for the new definition is that the t_{rise} and t_{fall} times in a regular ECL circuit are asymmetric with the delay dominated by $t_{fall} > t_{rise}$ The critical improvement is really in the t_{fall} time and we have chosen to emphasize this improvement by taking the worse delay, rather then to diminish its effect by taking an average value.

The sensitivity to capacitive load exhibited by the new ECL gate as compared to [1], [6] and [7] is shown in Fig. 7.

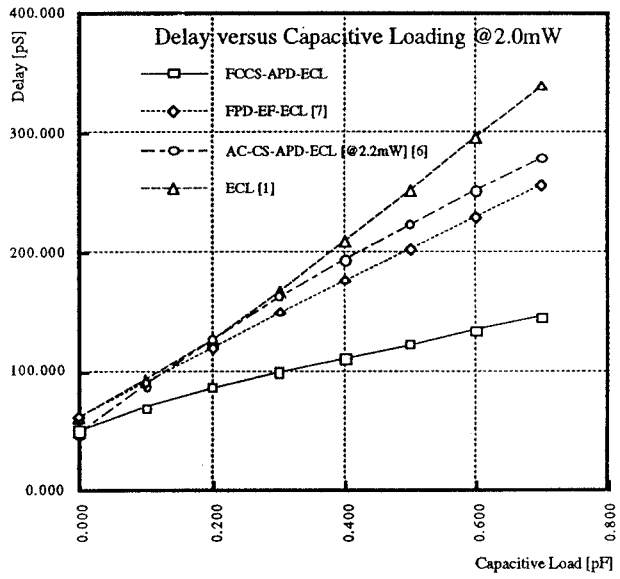


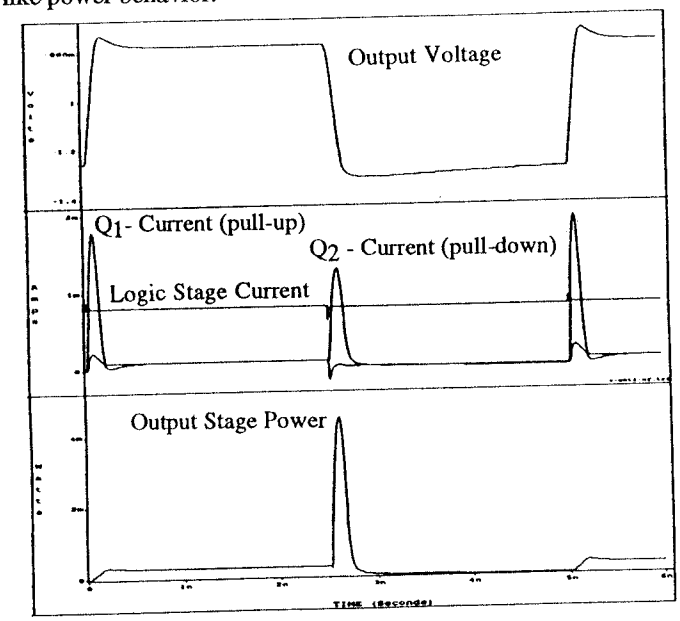
Fig. 7. *Delay versus capacitive loading for ECL [1], AC-CS-APD-ECL [6], FPD-EF-ECL [7] and FCCS-APD-ECL*

The superior load driving capability of FCCS-APD-ECL is visible from Fig. 7 and the specific data is shown in Table 2 for the 2.0 mW per gate power.

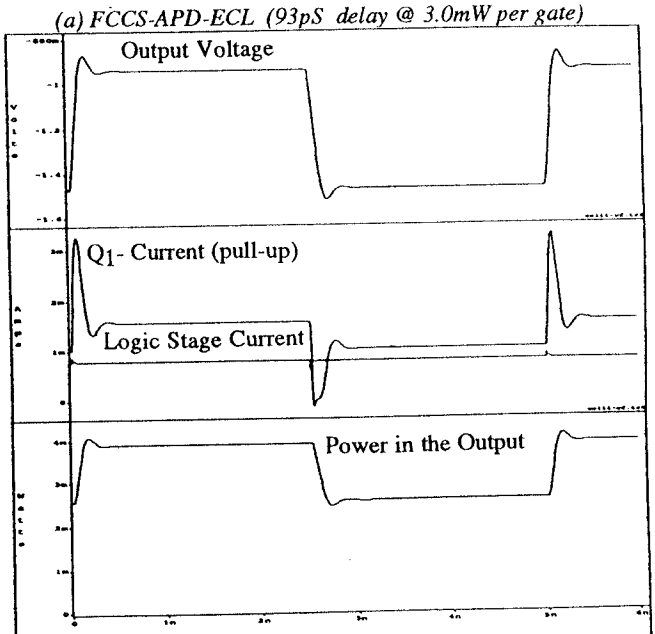
Table 2: Driving Capability at 2.0 mW per gate power

FCCS-APD-ECL	133pS/pF
FPD-EF-ECL [8]	276pS/pF
AC-CS-APD-ECL [7]	328pS/pF
ECL [1]	403pS/pF

The advantage of the new circuit over its counterparts is shown by the output current waveforms. A typical simulated voltage, current and output power waveforms for our circuit (a) compared to regular ECL [1] (b) are shown in Fig. 8. During the *steady state* intervals the current in our circuit is very small compared to the others. On the contrary, during the transitions our circuit exhibits large current peaks which are responsible for its excellent driving ability. The power generated in the output stages is shown in (c). When averaged over the signal interval it is substantially smaller than [1,6-7] which explains its CMOS like power behavior.



(a) FCCS-APD-ECL (93pS delay @ 3.0mW per gate)



(b) ECL [1] (93pS delay @ 5.6mW per gate)

Fig. 8 *Simulated output voltage, current and power response for the square pulse at the input, for FCCS-APD-ECL versus [1] using 0.3 pF load*

5. CONCLUSION

The new ECL circuit (FCCS-APD-ECL) shows advantage in low power consumption over the ones previously reported [3-8] yet maintaining the speed. This is achieved by a combination of controlled current source and careful tuning of signal levels and their timing relationship resulting in increased dynamic and reduced static current in the output stage. Therefore the major part of the power budget is consumed in the logic stage rather than the output stage, which sets this circuit apart from the previously developed ones. The ability of this circuit to handle higher capacitive loads is particularly important and offsets its inability for *wired-OR*. This is the main disadvantage of this gate compared to the FPD-EF gate [7], which has remarkably simple structure. The power consumed in the logic part is common to all ECL circuits. Developing circuit techniques which will reduce the power in the logic part is an important and promising area for future work.

Acknowledgment

The author is grateful to Sun Microsystems Laboratories which has provided support and stimulating environment, especially to George Taylor, Paul Hansen, Gary Bewick, Mark Santoro and Lee Tawrov for many helpful discussions. Support from the Office of Research of the University of California Davis is gratefully acknowledged as well as help provided by my students Yiding Gu and Alan Shih.

REFERENCES

[1] H.J.Greub et al, "*High-Performance Standard Cell Library and Modeling Technique for Differential Advnced Bipolar Current Tree Logic*", IEEE Journal of Solid State Circuits, Vol.26, No.5, May 1991.

[2] N. Jouppi et al, "*A 300MHz 115W 32b Bipolar ECL Microprocessor with On-Chip Cache*", Digest of Technical Papers, IEEE 40th International Solid-State Circuit Conference, San Francisco, February 24-26, 1993.

[3] C.T.Chuang, "*Advanced Bipolar Circuits*", IEEE Circuits and Devices Magazine, November 1992.

[4] K. Toh et al, "*A 23-pS / 2.1-mW ECL Gate with an AC-Coupled Active Pull-Down Emitter-Follower Stage*", IEEE Journal of Solid-State Circuits, Vol.24, No.5, October 1989.

[5] C.T.Chuang et al, "*High-Speed Low-Power AC-Coupled Complementary Push-Pull ECL Circuit*", IEEE Journal of Solid-State Circuits, Vol.27, No.4, April 1992.

[6] C.T.Chuang et al, "*High-Speed Low-Power ECL Circuit with AC-Coupled Self-Biased Dynamic Current Source and Active-Pull-down Emitter-Follower Stage*", IEEE Journal of Solid-State Circuits, Vol.27, No.8, August 1992.

[7] H. J. Shin, "*Self-Biased Feedback-Controlled Pull-Down Emitter Follower for High-Speed Low-Power Bipolar Logic Circuits*", 1993 Symposium on VLSI Circuits, Digest of Technical Papers, p.27, Kyoto, JAPAN, May 19-21, 1993.

[8] Tadahiro Kuroda, et al, "*Capacitor-Free Level-Sensitive Active Pull-Down ECL Circuit with Self-Adjusting Driving Capability*", 1993 Symposium on VLSI Circuits, Digest of Technical Papers, p.29, Kyoto, JAPAN, May 19-21, 1993.

[9] Tadahiro Kuroda, "*BiCMOS - Where is the Beef*", Panel Discussion, 1993 Symposium on VLSI Circuits, Kyoto, JAPAN, May 19-21, 1993.

[10] M. Hiraki, et al, "*A 1.5V Full-Swing BiCMOS Logic Circuit*", IEEE Journal of Solid State Circuits, Vol.27, No. 11, November 1992.

[11] V. G. Oklobdzija, "*New ECL Gate in BiFET Process*", Electronics Letters, Vol. 29, No. 23, November 1993.