New ECL gate in BiFET process

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Indexing terms: Emitter-coupled logic, BiCMOS integrated circuits

An ECL gate implemented as a combination of bipolar and MOS circuits in a BiFET process is presented. The resulting ECL gate exhibits an improved speed-power product over circuits presented in the past. Owing to its reduced power consumption this gate allows a higher level of integration for ECL. The process used is standard BiCMOS.

Introduction: In very high-performance VLSI systems ECL has attracted renewed attention and shown new promise. The critical issue is to reduce the power and yet preserve the driving capabilities and switching speed.

Advantages of using ECL are:

(1) switching current in a bipolar differential pair is a much faster operation than can be achieved with MOS transistors

(2) the voltage swing of the signal propagated through the wire is much smaller than in a comparable CMOS structure; the reduced voltage swing helps in reducing the propagation delay as well as the power consumption given that the dynamic portion of the power consumed in the chip is

$$P_0 = f_0 C_L V_S^2$$

In a regular ECL gate the switching speed is determined by the value of the resistor in the path to ground. There is a direct relation between the static and dynamic current. Any increase in the dynamic current results in more power being consumed by the gate.

Researchers from IBM have developed several very clever ECL structures using a push-pull bipolar combination in the output [1–3]. In their structures a path is provided from the logic tree of the ECL structure to the 'pull-down' output transistor resulting in an extra amount of charge being injected into its base when needed to speed up the transition. Their circuit results in faster operation at lower power, compared to regular ECL, most notably the circuit developed by Shin of IBM termed FPD-FF-ECL [4]. This circuit has remarkable simplicity while yielding several benefits such as the ability to permit 'emitter doting'.

However, reported schemes were not able to reduce the static current in the output stage, because any subsequent reduction would result in a lowering of the driving capability and in turn the speed of the gate. The operation of AC-APD-ECL of IBM [3] is shown in Fig. 1.

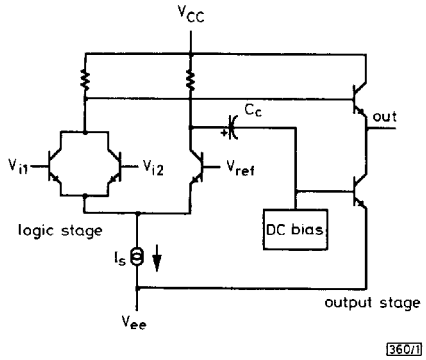

Fig. 1 *AC-ADP-ECL from IBM [3]*

Circuit operation: Operation of our circuit is summarised in Fig. 2which illustrates the major parts of this circuit. The circuit consists of an ECL logic tree (1), controlled current source (2), output driver stage (3) (consisting of the transistors Q_1 and Q_2) and feedback stage (4). The current source is controlled by the logic stage as well as the feedback stage. The phasing of the signals occurs in such a way that the current source is producing its maximally available current during the high-to-low transition of its output stage. During the low to high transition, as well as in the steady state the current source is in the reduced current mode providing just enough current to keep the transistor in slightly conducting mode.

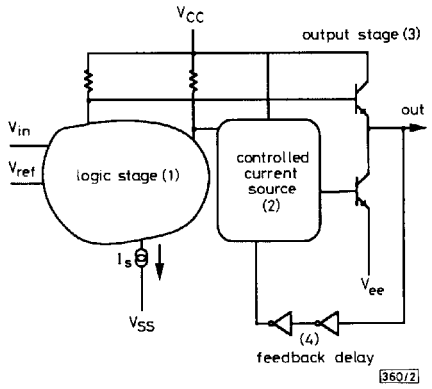

Fig. 2 *Circuit operation*

This ensures sufficient current drive for the output transistor Q_2 to discharge the load capacitance C_L and drive the output node from the 'high' to 'low' state. Output transistor Q_1 is driven directly from the logic stage. The current source (2) is driven by two opposite phases. First the current in the 'current mirror' is provided by the logic stage (1) in opposite phase to the stage driving output transistor Q_2. This ensures that transistors Q_1 and Q_2 are driven in opposite phases thus eliminating the direct current path from V_{cc} to V_{ee}.

Low to high transition of the output stage is achieved by driving Q_1. During this transition, the current source which drives Q_2 is set to low current because of the output being low. This enables fast low to high transition. The output node reaches the high value and after a delay through the feedback path (4) the controlled current source (2) will be enabled for high current. However, the input from the logic stage (1) keeps the controlled current source in the low current mode.

During a high to low transition, the signal from the logic (1) sets the current source (2) to high current. This results in high current driving the transistor Q_2 and thus resulting in a fast transition from high to low at the output. After this transition occurs and after delay in the feedback stage (4) the controlled current source (2) will reduce the current driving Q_2 and set the stage for the low to high transition. The delay introduced by the feedback stage is necessary to assure sufficient driving current during the transitions. The full circuit is shown in Fig. 3. In this case feedback delay (4) is realised using the RC delay of resistor R_f and the gate capacitance of transistor MN2.

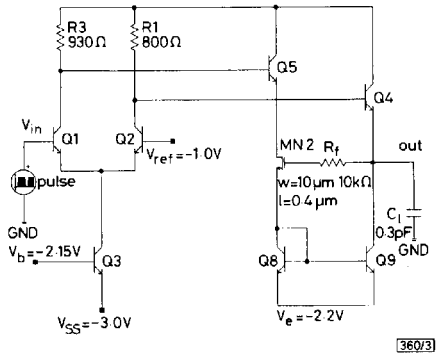

Fig. 3 *New ECL-CMOS gate*

Conclusion: This new ECL gate operates faster than those reported in [1–4]. At a gate power of 2mW and output load of

0.3pF the delay of the new gate is 101ps as opposed to 166ps of regular ECL, 148ps of [4] and 153ps of [3], which is obtained by simulation using our transistor models.

The power consumption of the new gate is lower than that of the reported gate. A 124ns delay is achieved with 1.23mW per gate against 2.82mW for the same delay in [4]. It is also significant that the power consumption of the new gate comes for the most part from its logic stage. The output stage has two orders of magnitude lower power consumption due to its complementary nature. Therefore this new gate has significantly higher driving capabilities.

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Wireless chip to chip interconnections for multichip modules using leaky wave antennas

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Indexing terms: Dielectric-loaded antennas, Integrated circuits

A novel interchip communication technique for very high speed multichip modules is presented. The feasibility of using a dielectric guide leaky wave antenna integrated on a chip for transmission and reception is discussed. J-band measurements and predictions based on a model developed using the transmission line matrix (TLM) method are compared.

Introduction: Multichip modules (MCMs) are receiving increasing attention as electronic equipment manufacturers move towards smaller and faster products. Advances in the performance of microelectronic devices for high speed computing and signal processing are limited by problems associated with interconnecting these devices to form multichip modules or systems [1]. Major bottlenecks in current metallic interconnects are propagation delays, reflections from discontinuities and crosstalk between adjacent signal lines [2]. This Letter proposes a novel means of chip to chip interconnection between devices in an MCM without taking signals through various discontinuities associated with metallic interconnects in the MCM substrate. In this method, communication between chips uses either quasioptical or millimetre wave signals.

Leaky wave antennas as radiative interconnects for MCMs: Beam steerable dielectric guide array antennas have been reported in the literature [3]. The design, fabrication and performance of dielectric waveguide technology for millimetre wave integrated circuits have also been demonstrated [4, 5]. Techniques to incorporate the radiating elements and feed lines on a monolithic chip [6, 7] have also been discussed. The concept combines these proven techniques to produce an interconnection system shown in Fig. 1. Communication between devices is via radiative beams reflected from the package lid. The inset shows the structure of the antenna used for measurements.

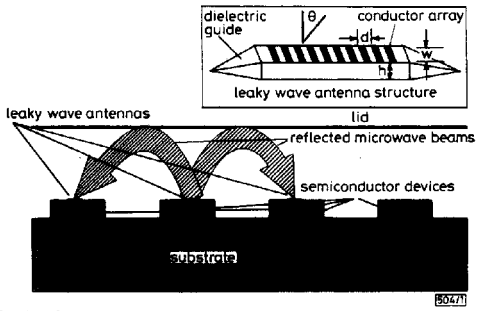

Fig. 1 *Schematic diagram of wireless interconnection system*

Despite the fact that the final system is intended to work at quasioptical frequencies, due to the availability of equipment, in this study low frequencies (J-band) were used.

Antenna structure design: The antenna consists of a dielectric (ε_r = 2.5) rectangular rod tapered at its ends, to give a matched connection to metallic waveguide, with an array of metallic elements on one side. Dielectric waveguide dimensions at the centre frequency (16GHz) were $w = 0.8\lambda_0$, $h = 0.38\lambda_0$. An array of 40 rectangular copper strips with $d = 0.4\lambda_0$ was attached to the top of the dielectric waveguide. The antenna was designed to produce a main beam at 45° from broadside, assuming that the radiated energy is due to the first backward spatial harmonic. The period of the array was calculated from [8].

Transmission line matrix (TLM) modelling.: Transmitting and receiving dielectric guide leaky wave antennas have been modelled using TLM-based field solving software. The near field intensities are obtained from the field solver, and Ludwig's third definition of crosspolarisation [9] is applied to these field components to find the copolar component of the electric field intensity. The far field patterns are then obtained using the electromagnetic equivalence principle [10]. The far field data are obtained from the TLM-generated near fields by computing the equivalent source current and vector potential [11]. Having obtained the far fields, the Poynting vector and power radiation pattern are determined.

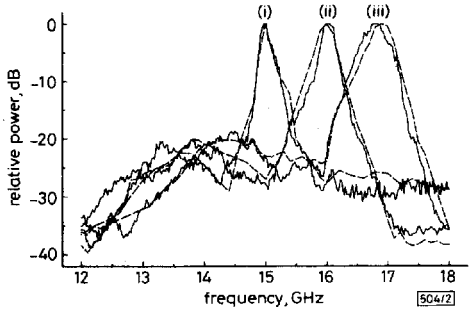

Fig. 2 Frequency response of receiving leaky wave antenna

(i) θ = –58°
(ii) θ = –43°
(iii) θ = –33°
– – – – modelled
——— measured

Measurements: In this study the dielectric waveguide was fed by metal waveguide. A waveguide load was used to ensure that VSWR was minimised. Frequency response measurements were made on the receiving antenna with signal incident at three differ-