Jitter Analysis of Nonautonomous MOS Current-Mode Logic Circuits

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***Abstract*—In this paper, we analyze the occurrence of jitter due to random and deterministic disturbances in nonautonomous current-mode logic circuits. First, we present an analytical model that explains the transformation of noise into jitter as a linear time-variant process, with its time-domain impulse response function and a frequency-domain system function. The model is then used to analyze jitter in two different circuits, with different sources of noise. In the first example, we use the model to predict jitter due to device noise in a frequency divider, and identify devices that are the main contributors to the jitter. In the second example, we examine jitter of a buffer with deterministic ground noise. Jitter predictions are compared to the results obtained through exhaustive simulation. According to the comparison, the method predicts jitter with an error of up to 3.4%.**

***Index Terms*—Integrated circuit design, jitter, modeling, noise.**

I. Introduction

In a most broad definition, term "jitter" refers to the dynamic uncertainty of the signal timing [1]. For an arbitrary digital signal, jitter represents a time-variant deviation of the times when the signal crosses a reference level. Hence, if the signal is differential, jitter is often defined as a variation of the zero-crossing times [2]. In the special case of periodic signals, jitter can also be defined as a variation of the signal period [3]. Then, deviation of the time difference between two signal transitions is observed, rather than a single edge. Uncertainty of the signal period can also be viewed in the frequency domain, and then it is referred to as phase noise.

Imperfect timing impacts the performance of both analog and digital systems: in wireless systems, jitter of the carrier causes interchannel interference and imposes limits on the minimum channel spacing [4]; in digital systems, clock jitter limits the maximum operable speed [1]; in communications systems, jitter causes synchronization problems and increases the bit-error rate [5], etc.

Jitter in integrated circuits is caused by various factors such as power supply noise, substrate noise, crosstalk, device noise, etc. Effects of some of these factors can be minimized by using appropriate design techniques and technological processes. For instance, jitter caused by power supply noise can be minimized by using differential signaling; jitter originating from substrate noise can be reduced by isolating devices and using a triple-well CMOS process. However, even with careful design, these noise sources will occur in any real system and will surely cause jitter. In addition, since device noise is intrinsic for any real circuit, jitter caused by device noise cannot be eliminated and it imposes a fundamental limit on the circuit performance [6]. Therefore, since it is inevitable in any real system, jitter and its origins need to be studied. Knowing the mechanisms by which noise transforms into jitter would be useful for several reasons. First, it would be possible to predict jitter before actually fabricating the circuit. Also, if we know how jitter is generated and how it depends on circuit parameters, we can reduce it by controlling these parameters.

A lot of research has been done on jitter and phase noise of integrated electric oscillators [2]–[9]. However, an oscillator is not the only source of jitter in a system. Other circuits (e.g., amplifiers, buffers, frequency dividers, etc.) can also introduce jitter and affect the performance of the system. Nonetheless, these circuits have not received as much attention in the literature. Some efforts include [10]–[12], which gave empirical phase noise models of frequency dividers, based on the experimental data available at the time. Recently, in [13], an analytical model that explained the transformation of random device noise into phase noise in frequency dividers was presented.

In this paper, we analyze the occurrence of jitter due to both random and deterministic disturbances in nonautonomous (driven) MOS current-mode logic (CML) circuits, which are commonly used in high-speed communications systems. First, we introduce a linear time-variant model that explains the transformation of noise into jitter. This analysis yields closed-form expressions, which are functions of circuit parameters and can be used to estimate jitter. Then, we demonstrate the method on two different CML circuits with different sources of noise. In the first example, we estimate jitter of a CML frequency divider with white and flicker device noise and identify the main jitter contributors in the circuit. In the second example, we analyze jitter due to deterministic ground noise in a CML buffer. Finally, we compare jitter estimates found in these two examples, with the results of exhaustive transient simulation in HSPICE.

II. Current-Mode Logic Circuit Design Technique

The process of noise transformation into jitter is closely related to the circuit topology. Therefore, before we start revealing

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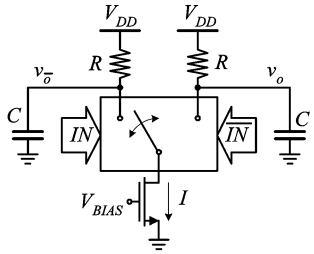

Fig. 1. Schematic of a general MOS CML gate.

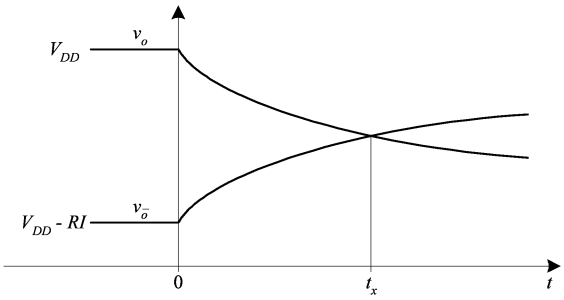

Fig. 2. Output waveforms of the CML gate from Fig. 1.

the mechanisms of jitter generation, we need to briefly explain the operation of MOS CML circuits [14].

Schematic of a generalized CML gate is given in Fig. 1. The nMOS pull-down network is controlled by the differential inputs, and it is used to steer the dc current I and produce the differential output. Capacitors C represent the total output capacitance, including the parasitics, and input capacitances of the subsequent gates. Timing diagrams of the outputs when they are switching are given in Fig. 2. The inputs change at time $t = 0$ and it is assumed that the entire current I is immediately steered through one of the two paths in the nMOS pull-down network (ideal switching). Consequently, output voltages follow the exponential function for $t \geq 0$:

$$v_o = V_{\rm DD} + RI\left(e^{-\frac{t}{RC}} - 1\right)$$
$$v_{\bar{o}} = V_{\rm DD} - RIe^{-\frac{t}{RC}} \quad (1)$$

and they cross at time $t = t_x$:

$$t_x = RC\ln 2. \quad (2)$$

Expression (2) gives the nominal crossing time, since it was derived in absence of any disturbance that could change the timing of the circuit.

III. The Model Used for Jitter Analysis

Our next goal is to study how the presence of a noise source (e.g., device noise, crosstalk, power supply noise, or any other type of disturbance) affects the nominal crossing time given by (2). This noise source can be represented by an equivalent current source $i(t)$, referred to the output of the circuit, as shown in Fig. 3. (Examples showing how different noise sources can be

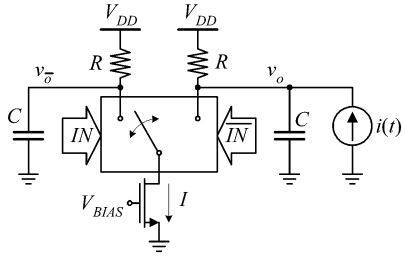

Fig. 3. A CML gate with a current source representing the equivalent output-referred noise.

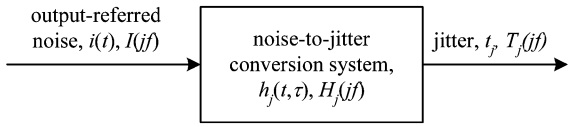

Fig. 4. Symbolic representation of the process of noise conversion into jitter.

referred to the output are presented in the Appendixes.) Now, it is sufficient to study how this single equivalent output-referred noise transforms into variations of the crossing time.

We will explain this phenomenon with an abstract system (or process), that we will call the noise-to-jitter conversion system, as illustrated in Fig. 4. We need to find an appropriate model for this system and determine whether it should be linear or nonlinear, time-variant or invariant. It is a reasonable assumption that noise can cause only small perturbations of voltages, and it cannot change the instantaneous operating point of the circuit [7]. In other words, at any time instant, the circuit can be linearized for the purpose of noise analysis [2], [6], [7]. Consequently, we can expect our noise-to-jitter system to be linear as well, and we can describe it with an impulse response function in the time domain, and a transfer function in the frequency domain. As we will see, describing the system in the frequency domain is of particular interest when dealing with random noise, since usually frequency-domain characteristics of noise are known (power spectral density, PSD), rather than its time-domain autocorrelation function. In addition to linearity, we can expect our model to be time-variant, since it is likely that effects of noise around the nominal crossing time are more pronounced than effects of noise long before (or after) the nominal crossing time. Therefore, we choose to define the model that describes the process of noise transformation into jitter as a linear time-variant process.

Before we start explaining the details of the noise-to-jitter conversion model, we should make one more remark. Unlike free-running oscillators, driven circuits do not exhibit jitter accumulation, i.e., their jitter does not increase with time. This is due to the existence of the input signal, which retimes the circuit with its each occurrence. As a consequence, phase noise of the circuits driven from periodic sources does not exhibit the $1/f^2$ behavior, which was confirmed in [10]–[13]. Hence, when analyzing how noise transforms into jitter in driven circuits, it is sufficient to observe this phenomenon around a single transition of the input signal, since previous crossing time variations do not affect the current one.

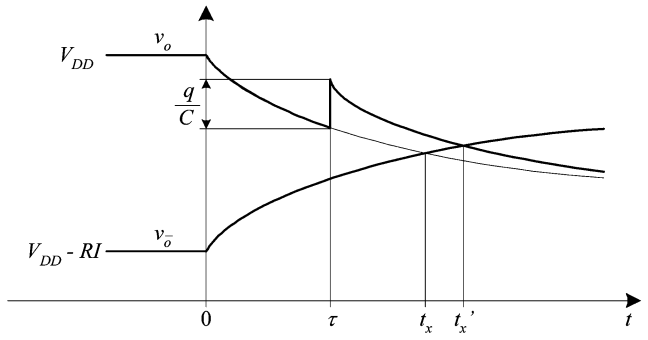

Fig. 5. Output waveforms of the CML gate from Fig. 3 when $i(t)$ is a current impulse arriving at $t = \tau$ and causing an abrupt increase of voltage v_o.

A. Jitter Model in the Time Domain and the Impulse Response Function

To describe the noise-to-jitter conversion system in the time domain, we need to find its impulse response function. Once we know that, we will be able to find the response of the system to any type of excitation, including random noise. In order to find the impulse response function, let us set the source $i(t)$ in Fig. 3 to be a current impulse arriving at $t = \tau$ (where $\tau \leq t_x$) and carrying a small electric charge of q coulombs: $i(t) = q \times \delta(t - \tau)$, where $\delta(t)$ is the Dirac impulse. (Note that the fact that q has to be small follows from the assumption that noise causes only small perturbations of the output voltages, which is a vital assumption for the conservation of linearity in our model.) The current impulse will cause an abrupt increase of voltage v_o by q/C volts at $t = \tau$, as depicted in Fig. 5. The effects of charge injection will diminish with time, following the exponential function. We can rewrite (1) with the new v_o:

$$\begin{aligned} v_o &= V_{\mathrm{DD}} + RI\left(e^{-\frac{t}{RC}} - 1\right) + (q/C)e^{-\frac{(t-\tau)}{RC}} \\ v_{\bar{o}} &= V_{\mathrm{DD}} - RIe^{-\frac{t}{RC}}. \end{aligned} \tag{3}$$

A new crossing time, t_x', can be found as

$$t_x' = RC\ln\left(2 + \frac{q}{IRC}e^{\frac{\tau}{RC}}\right). \tag{4}$$

By subtracting (2) from (4), and using $\ln(1 + x) \approx x$ for a small x, which is a valid approximation since we assumed that the charge injected by the source is very small, variation of the crossing time caused by the charge injection at time $t = \tau$ can be found as

$$\Delta t_x(\tau) = t_x' - t_x = \frac{q}{2I}e^{\frac{\tau}{RC}}. \tag{5}$$

Dividing $\Delta t_x(\tau)$ by q, from (5) we can obtain a function which shows the dependence of the crossing time variation on the arrival time of the unit current impulse. In [7], a similar function was referred to as the impulse sensitivity function (ISF), $\Gamma(\tau)$. We will adopt this term and use it throughout this paper. (In [7], ISF represents the phase shift due to a current impulse, observed in an oscillator after several cycles of the output signal, i.e., after the system reaches its steady state. Here, ISF represents crossing time variation due to charge injection during the transients. Also, in [7], ISF is obtained through simulation, while here we compute it analytically.)

In the analysis above, we assumed that the current impulse causing the crossing time variation arrived at time $\tau \leq t_x$. If the impulse arrives after the outputs have already crossed ($\tau > t_x$), this charge injection could potentially cause additional crossings of the outputs. However, in our analysis, we observe only the first signal crossing, while ignoring any consecutive bouncing of the outputs. (This is known as the first-crossing approximation [9]). Therefore, for the purpose of our analysis, impulses arriving after the nominal crossing time have no effect on jitter. With this in mind, we can now complete the definition of the ISF:

$$\Gamma(\tau) = \begin{cases} \frac{1}{2I}e^{\frac{\tau}{RC}}, & \text{for } \tau \in (-\infty, t_x] \\ 0, & \text{for } \tau > t_x. \end{cases} \tag{6}$$

Finally, we can define the impulse response function of the noise-to-jitter conversion system, $h_j(t, \tau)$, as

$$h_j(t, \tau) = \Gamma(\tau) \times u(t - \tau) \tag{7}$$

where $u(t)$ is the unit step function. The unit step function indicates that effects of charge injection around the crossing accumulate: crossing time will be affected by all instances of charge injection that occurred prior to the time of observation.

Substituting $\Gamma(\tau)$ from (6), (7) becomes

$$h_j(t, \tau) = \begin{cases} \frac{1}{2I}e^{\frac{\tau}{RC}}u(t - \tau), & \text{for } \tau \in (-\infty, t_x] \\ 0, & \text{for } \tau > t_x. \end{cases} \tag{8}$$

It can be seen from (8) that, since the impulse response of the noise-to-jitter conversion system depends on the arrival time of the input τ, the system is time-variant (LTV).

Now that we have defined the impulse response function, we can use the convolution integral, which holds for any linear system, to find jitter caused by an arbitrary deterministic disturbance signal $i(t)$:

$$t_j(t) = \int_{-\infty}^{+\infty} h_j(t, \tau)i(\tau)d\tau. \tag{9}$$

Note that, the way we defined it in (9), jitter is a function of time. Since jitter is a variation of the crossing time, we should evaluate (9) at the nominal crossing time, t_x [even though, because of the definition of $h_j(t, \tau)$ in (8), the same result would be obtained if (9) were evaluated for any $t > t_x$]. With this in mind, and using the noise-to-jitter impulse response function from (8), we can find jitter as

$$t_j = t_j(t_x) = \frac{1}{2I}\int_{-\infty}^{t_x} e^{\frac{\tau}{RC}}i(\tau)d\tau. \tag{10}$$

Equation (10) can be used to find deterministic jitter, when $i(t)$ is known. However, in case when $i(t)$ represents random noise, its amplitude is arbitrary and the signal is characterized by its autocorrelation function, $R_i(t, \xi)$, rather than its instantaneous values. Crossing time variations caused by this random signal are also random, and (10) is not applicable anymore.

We can use another form of the convolution integral, valid for random signals, to find the autocorrelation of jitter $R_j(t,\xi)$ [15]:

$$R_j(t,\xi) = \int_{-\infty}^{+\infty}\int_{-\infty}^{+\infty} h_j(t,r)h_j(\xi,s)R_i(r,s)\,dr ds. \tag{11}$$

When jitter is random, its instantaneous value is unknown, but we can find its root-mean-square (rms) value. In order to do so, we need to evaluate (11) at $t=\xi$ and thus obtain the jitter variance (or power). The rms value can then be found by finding the square-root of the variance. (Here, we are assuming that the output-referred noise is a stationary random process with a zero mean. Therefore, jitter is also a stationary process with a zero mean, and its variance is equal to its autocorrelation with a zero shift. Power, on the other hand, is equal to the variance [15].) Just like we did in case of deterministic jitter in (10), since jitter represents a variation of the crossing time t_x, we should evaluate (11) at $t=\xi=t_x$. Therefore, if we substitute $h_j(t,\tau)$ from (8) into (11), jitter variance at the nominal crossing time can be found as

$$\begin{aligned}\sigma_j^2 &= \sigma_j^2(t_x) = R_j(t_x,t_x)\\ &= \frac{1}{4I^2}\int_{-\infty}^{t_x} e^{\frac{s}{RC}}\left\{\int_{s}^{t_x} e^{\frac{r}{RC}}R_i(r,s)dr\right\}ds\end{aligned} \tag{12}$$

and its rms value is the square-root of the above expression.

At this point, assuming circuit parameters are also known, we can determine jitter of the CML gate, if we know the exact time function of the source $i(t)$ (when it is a deterministic signal), or its autocorrelation (when it represents random noise), by using (10) or (12), respectively. For instance, let us assume that the only disturbance that can affect the timing of the CML gate is the thermal noise of the resistor R connected to the v_o output of the circuit. Then, we can find the autocorrelation function of the source $i(t)$ to be [16], [17]

$$R_i(t,\xi) = \frac{2kT}{R}\times\delta(t-\xi). \tag{13}$$

Substituting (13) into (12), (12) becomes

$$\sigma_j^2 = \frac{kT}{2RI^2}\int_{-\infty}^{t_x} e^{\frac{2s}{RC}}ds. \tag{14}$$

Finally, using the value for t_x from (2), variance of jitter caused by the thermal noise of the output resistor R is

$$\sigma_j^2 = \frac{kTC}{I^2}. \tag{15}$$

The equation above gives a known expression for jitter when only white thermal noise is present in the circuit, and it can alternatively be derived by dividing the thermal noise power kT/C by the square of the output signal slope at the nominal crossing time $(I/C)^2$ [6], [13].

Equation (12) can be used to compute jitter power for any CML circuit, with any type of noise whose autocorrelation is known. It is particularly convenient when only white noise is present, since white noise is uncorrelated and its autocorrelation function will be in the form of an impulse, just like in (13). However, in case of $1/f$ (flicker) noise, autocorrelation function is not an impulse anymore, and hand-computation of (12) becomes cumbersome. In general, rather than autocorrelation, PSD of noise is given, and hence it would be much more convenient to have a frequency-domain model of the noise-to-jitter conversion system in order to find jitter due to both white and $1/f$ noise.

B. Jitter Model in the Frequency Domain and the System Function

In case of a linear time-invariant (LTI) system, transfer function can be found as the Fourier integral of the impulse response function. Similarly, a system function (time-variant transfer function) can be defined for an LTV system as [18]

$$H(jf,t) = \int_{-\infty}^{+\infty} h(t,\tau)e^{-j2\pi f(t-\tau)}d\tau$$

with

$$f\in(-\infty,\infty) \tag{16}$$

where $h(t,\tau)$ is the impulse response function of the given LTV system. If we apply (16) to the impulse response function of our noise-to-jitter conversion system defined in (8), we get

$$H_j(jf,t) = \int_{-\infty}^{\min\{t,t_x\}} \frac{e^{\frac{\tau}{RC}}}{2I}e^{-j2\pi f(t-\tau)}d\tau,$$

where

$$f\in(-\infty,\infty). \tag{17}$$

In this way, we obtained a system function, $H_j(jf,t)$, which characterizes the noise-to-jitter conversion system in the frequency domain.

Since we are interested in finding jitter, which is the variation of the signal crossing time, we want to know the system function at the nominal crossing time and therefore we should evaluate (17) at $t=t_x$. Substituting t_x from (2) into (17) and performing the integration, we obtain the final expression for the system function of the noise-to-jitter conversion system:

$$H_j(jf,t_x) = \left(\frac{RC}{I}\right)\frac{1}{1+(j2\pi RCf)}$$

where

$$f\in(-\infty,\infty). \tag{18}$$

Now, we can find the Fourier transform of jitter, $T_j(jf)$, if we know the Fourier transform of the source $i(t), I(jf)$:

$$\begin{aligned}T_j(jf) &= H_j(jf,t_x)\times I(jf)\\ &= \left(\frac{RC}{I}\right)\frac{I(jf)}{1+j2\pi fRC}.\end{aligned} \tag{19}$$

Jitter can then be found by performing the inverse Fourier transform on (19), which should yield the same result as the one obtained in the time domain, given by (10).

Expression (19) can be used to find deterministic jitter in the frequency domain. However, when $i(t)$ represents noise, its PSD $S_i(f)$ (i.e., the Fourier transform of the autocorrelation $R_i(t,\xi)$) will be given, rather than $I(jf)$. Then, the PSD of jitter $S_j(f)$ can be found as [15]

$$S_j(f) = |H_j(jf, t_x)|^2 S_i(f). \tag{20}$$

The variance (power) of jitter can now be calculated as the integral of the jitter PSD in (20), over all frequencies:

$$\sigma_j^2 = \int_{-\infty}^{+\infty} |H_j(jf, t_x)|^2 S_i(f) df. \tag{21}$$

Substituting (18) into (21), an expression that gives variance of jitter of a CML gate with output-referred noise whose PSD is $S_i(f)$ can be obtained:

$$\sigma_j^2 = \left(\frac{RC}{I}\right)^2 \int_{-\infty}^{+\infty} \frac{1}{1+(2\pi fRC)^2} S_i(f) df. \tag{22}$$

Expression (22) can be used to find the power of random jitter, and its rms value can be found as the square root of (22).

According to Parseval's theorem, jitter power in the frequency domain, expressed in (22), will be the same as jitter power found in the time domain, given by (12). To demonstrate the equality between jitter models in the time and frequency domains, let us use the frequency-domain model to find jitter caused by the thermal noise of the output resistor of the CML gate, R, as we did earlier in the time domain. In this case, single-sided PSD of the output-referred noise is [16]

$$S_i(f) = \frac{4kT}{R}, \text{where } f \in [0, \infty). \tag{23}$$

It can be shown that, by substituting (23) into (22), jitter variance is

$$\sigma_j^2 = \frac{kTC}{I^2} \tag{24}$$

which is the same as the result we found in the time domain, (15).

Equation (22) allows us to find jitter power of a CML circuit with any type of output-referred noise, as long as its PSD is known. In general, output-referred noise of a MOS CML circuit will consist of flicker and white noise, and its single-sided PSD will be of the form

$$S_i(f) = \frac{K_F}{f} + K_W, \text{with } f \in (f_L, f_H) \tag{25}$$

where K_F and K_W are flicker and white noise parameters which depend on circuit topology and bias conditions, and f_L and f_H are the lower and upper limits of the bandwidth of interest. (Note that f_L has to be greater than zero, otherwise noise power could be infinite on a finite frequency interval $f_H - f_L$.) If we substitute this general PSD into (22), with the integration boundaries being f_L and f_H, we can derive a closed-form expression that gives jitter variance of a CML circuit in presence of $1/f$ and white noise at one of its outputs:

$$\sigma_j^2 = \left(\frac{RC}{I}\right)^2 \left\{ K_F \ln\left(\frac{f_H}{f_L}\sqrt{\frac{1+(2\pi RCf_L)^2}{1+(2\pi RCf_H)^2}}\right) + \frac{K_W}{2\pi RC}\left(\arctan(2\pi RCf_H) - \arctan(2\pi RCf_L)\right)\right\}. \tag{26}$$

The rms value of jitter can be found as the square root of the above expression:

$$\sigma_j = \left(\frac{RC}{I}\right) \left\{ K_F \ln\left(\frac{f_H}{f_L}\sqrt{\frac{1+(2\pi RCf_L)^2}{1+(2\pi RCf_H)^2}}\right) + \frac{K_W}{2\pi RC}\left(\arctan(2\pi RCf_H) - \arctan(2\pi RCf_L)\right)\right\}^{\frac{1}{2}}. \tag{27}$$

Note that, when there is no $1/f$ noise in the circuit, i.e., $K_F = 0$, and the only source of device noise is the thermal noise, with $K_W = 4kT/R$, if we let $f_L = 0$ and $f_H \to \infty$, expression (27) reduces to (15), i.e., (24).

Since, in most practical cases, PSD of the output-referred noise is given, rather than its autocorrelation, (27) and (26) will be used much more often than (12), which calculates jitter in the time-domain.

IV. Verification of the Model and Jitter Analysis Examples

In this section, we will use the method described above to estimate jitter in two cases of different CML circuits with different sources of noise. In the first example, we will analyze random jitter of a frequency divider, caused by device noise originating from the transistors comprising the circuit. In the second example, we will estimate deterministic jitter of a CML buffer, caused by the ground conductor noise. Jitter estimates in both cases are compared to the results of the exhaustive transient HSPICE simulation.

A. Random Jitter of the CML Frequency Divider Caused by Device Noise

Frequency dividers are inevitable parts of high-frequency phase-locked loops (PLL) and their contribution to the PLL output jitter can be very significant, especially as the PLL frequency multiplication factors increase [19]. Some other applications of frequency dividers include communications systems which employ the serialize-deserialize (SERDES) algorithms. In these systems, frequency dividers are used to generate multirate clocks for the serializer in the transmitter, and the deserializer in the receiver. Hence, in this case, jitter of frequency dividers directly translates into clock jitter.

CML frequency dividers are constructed as asynchronous counters. Schematic of a one-stage divider (divider by two) is shown in Fig. 6: it consists of a master-slave latch, connected as a T-flip-flop. The outputs of the circuit toggle after each rising edge of v_{in}. Relevant circuit parameters which will be used for jitter estimation are summarized in Table I. I is the dc bias current, R represents the equivalent output resistance of a

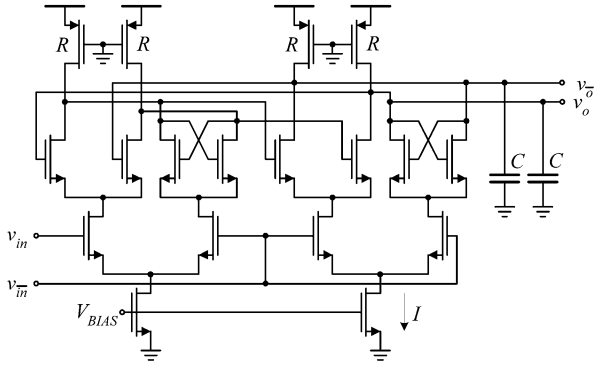

Fig. 6. Schematic of the one-stage MOS CML frequency divider.

latch (primarily due to the active pMOS load) and C represents the total output capacitance of the slave latch, including gate capacitance of the master latch, parasitics of the slave latch, as well as any additional output load capacitance.

With no other noise sources present, timing jitter of the frequency divider output signal will be caused by device noise. It is important to note that only device noise originating from the slave latch will affect the timing of the circuit: at the time when outputs of the divider (i.e., slave latch) are switching, outputs of the master latch are stable and therefore, noise from the master latch cannot affect the timing of the divider output [13]. PSD of the output-referred noise of the slave latch was found to be of the form expressed in (25), with flicker and white noise coefficients:

$$K_F = 2.6 \times 10^{-15}\ \mathrm{A}^2$$
$$K_W = 4.1 \times 10^{-23}\ \mathrm{A}^2/\mathrm{Hz}. \tag{28}$$

These coefficients can be determined either through HSPICE or analytically, as explained in Appendix A. It should be noted that this PSD corresponds to the noise at only one output of the slave latch (more precisely, the output that is performing the high-to-low transition). At the other output of the latch, noise with a different PSD will exist, as shown in Appendix A. However, in the simulations carried out in order to verify our jitter model and in the analysis that follows, we will assume that only one source of noise exists at one output of the circuit, and its PSD is given by (25), with coefficients K_F and K_W from (28). In other words, we are creating the situation depicted in Fig. 3, with a frequency divider circuit instead of the general CML gate, and a noise source $i(t)$ whose PSD is given by (25) and (28). For now, we are ignoring the noise source at the other output of the frequency divider since, at this point, our main goal is to reveal the mechanisms of noise conversion into jitter, rather than find the exact value of noise and/or jitter. Once we have confirmed that our model is valid, we will easily find more refined estimates of jitter, with all noise sources considered.

With this in mind, let us apply (27), with circuit parameters given in Table I, noise coefficients (28) and bandwidth boundaries $f_L = 1$ Hz and $f_H = 100$ GHz, and estimate jitter of the frequency divider. (The upper frequency f_H was chosen so that the magnitude of the noise-to-jitter system function (18) becomes negligible beyond f_H. The lower frequency f_L was chosen so that condition $f_L > 0$ is satisfied.) Finally, the estimated rms jitter of the frequency divider circuit is

TABLE I
PARAMETERS OF THE CML FREQUENCY DIVIDER FROM FIG. 6, USED IN JITTER CALCULATIONS

Parameters	Units	Values
I	[μA]	315
R	[kΩ]	1.25
C	[fF]	34.5
t_x (=RCln2)	[ps]	30

$$\sigma_{j1} = 73.6\ \mathrm{fs}. \tag{29}$$

This result is now compared to the result obtained through exhaustive transient simulation in HSPICE. To simulate noise in HSPICE, the method applied in [20] is used: a piecewise linear (PWL) current source is connected to one output of the CML frequency divider, as shown in Fig. 3. Instantaneous values of this PWL source are pseudorandom and determined using MATLAB so that the PSD of the source matches the calculated PSD of the output-referred frequency divider noise, given by (25) and (28). Fig. 7 shows the comparison between the PWL source PSD (gray line), and the calculated PSD (black line). A simple analysis in MATLAB shows that the average error between these two PSDs is very small (less than 0.1%), which is not surprising since the PWL sequence is determined using the coefficients of the calculated PSD.

To create a time-domain sequence for the PWL source, whose PSD contains both $1/f$ and white components, the sequence is divided into two subsequences. The PSD of the first one is white, and its instantaneous values are obtained using the pseudorandom number generator embedded in MATLAB, with the desired variance K_W specified in (28). The time step of this sequence (1 ps) needs to be much smaller than the RC constant of the frequency divider circuit (43 ps), so that the sequence has a white PSD over the entire bandwidth of interest, as suggested in [20]. The other subsequence, which has a $1/f$ PSD, is created using the method proposed in [21]: based on the fact that $1/f$ noise belongs to the class of self-similar processes, a discrete-time filter whose frequency response has an $f^{-1/2}$ characteristic can be designed. The $1/f$ subsequence, with the coefficient K_F from (28), is then obtained by passing a white sequence through this filter. Finally, the two subsequences are added together in the time domain to form the PWL sequence, whose PSD is shown in Fig. 7 (gray line). Since the subsequences are mutually uncorrelated, the resulting PSD is a sum of the PSDs of the two subsequences, and it hence contains $1/f$ and white regions.

The frequency divider circuit is simulated with the PWL source described above at its output for 1000 periods of the output signal. A long simulation stop time (1 μs) is needed to observe effects of the slowly-varying $1/f$ noise. Simulation step time has to be kept very small (10 fs), so that even small variations of the crossing times can be observed. With these simulation parameters, total simulation time is around 28 hours on a Sun machine with 1.1-GHz Sparc V9 processor and 1 GB of RAM, running Solaris 8 OS. Variations of the crossing times

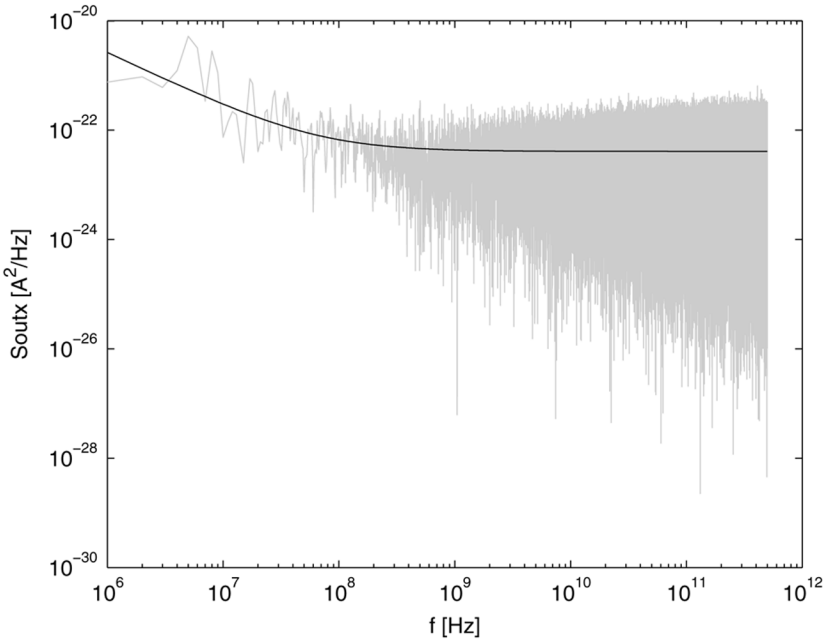

Fig. 7. Comparison of the calculated PSD of the output-referred frequency divider noise (black line), and the PSD of the sequence which represents the instantaneous values of the PWL current source used to simulate noise in the HSPICE transient simulation (gray line).

caused by the presence of the PWL source are recorded and their standard deviation is found to be

$$\sigma_{j1,\mathrm{HSPICE}} = 74.5 \text{ fs}. \tag{30}$$

When this is compared to the estimated rms jitter given in (29), it can be seen that our noise-to-jitter conversion model predicts the simulated jitter with an accuracy of 1.2%, which allows us to conclude that our method closely models the process of noise conversion into jitter.

For the sake of completeness, now that we have verified our model, we can find a more realistic estimate of the frequency divider jitter if we include the noise that occurs at the other output of the circuit. As shown in Appendix A, output-referred noise at the output performing the low-to-high transition has noise coefficients:

$$\begin{aligned} K_F &= 1.9 \times 10^{-15}\ \mathrm{A}^2 \\ K_W &= 1.4 \times 10^{-23}\ \mathrm{A}^2/\mathrm{Hz}. \end{aligned} \tag{31}$$

With these coefficients, and frequency limits $f_L = 1$ Hz and $f_H = 100$ GHz, (27) yields

$$\sigma_{j2} = 43 \text{ fs}. \tag{32}$$

Since, as explained in Appendix A, noise sources at the two outputs of the frequency divider are uncorrelated, the total rms jitter of the frequency divider is estimated to be

$$\sigma_{j,\mathrm{tot}} = \sqrt{\sigma_{j1}^2 + \sigma_{j2}^2} = 88 \text{ fs}. \tag{33}$$

Finally, let us use (27), together with the results presented in Appendix A, to identify the most significant contributors to the frequency divider jitter. First, if we apply (27) with $1/f$ noise coefficients $K_F = 0$ and white noise coefficients K_W from (28) and (31), jitter of the frequency divider differential output turns out to be around 78 fs. Comparing this to the total jitter given in (33), it can be concluded that most of the jitter comes from the white noise sources, while only a smaller amount of jitter is due to flicker noise. Next, by observing the values for β (current gains from individual device noise sources to the output) found in Appendix A, we see that only the tail current source m_1, as well as the pMOS load transistors m_4 and m_5, practically contribute to the output noise. On the other hand, effects of the clock and data transistors m_2 and m_3 on the output noise are significantly attenuated. Moreover, by applying (27) to individual noise sources, it can be shown that load transistors m_4 and m_5 cause about one half of the total jitter, while the current source m_1 contributes the other half.

B. Deterministic Jitter of the CML Buffer Caused by the Ground Noise

In the second experiment, we will study how variations of the ground voltage affect the crossing times of the CML buffer outputs. We will assume that the ground voltage variation can be modeled as a deterministic disturbance that occurs with some known period. This voltage disturbance may have been caused, for example, by the switching of some digital circuitry, which is connected to the same ground line as the buffer. The equivalent schematic of the CML buffer with the ground noise source is shown in Fig. 8, and relevant circuit parameters are given in Table II.

Let us assume that one period of the ground noise signal can be modeled as a pulse with an amplitude of V_n volts, occurring at $t = t_0$ and lasting for t_x seconds, where t_x is the nominal

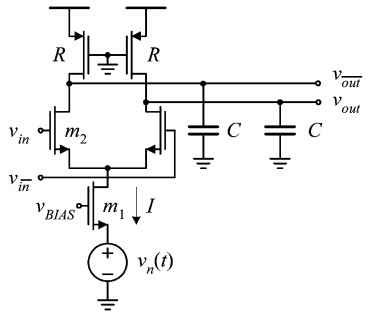

Fig. 8. Schematic of the CML buffer with a voltage source, $v_n(t)$, representing the ground noise.

TABLE II
PARAMETERS OF THE CML BUFFER FROM FIG. 8, USED IN JITTER CALCULATIONS

Parameters	Units	Values
I	[μA]	315
R	[kΩ]	1
C	[fF]	30
t_x (=RCln2)	[ps]	20

crossing time (or delay) of the buffer outputs, whose value is given in Table II. Therefore, one pulse of $v_n(t)$ is

$$v_n(t) = V_n[u(t-t_0) - u(t-t_0-t_x)] \tag{34}$$

where $u(t)$ is the unit step function. Let the period of the ground noise signal be equal to or greater than the period of the buffer output signal. With this assumption, any observed crossing time of the buffer outputs will be affected by only one noise pulse (34), arriving right prior to that crossing. In the following analysis, our goal is to find the worst-case jitter caused by one such pulse, $|t_j|_{\max}$.

In order to find jitter caused by the ground noise, $v_n(t)$ needs to be referred to the output of the CML buffer and represented by an equivalent current source $i(t)$, as in Fig. 3. As shown in Appendix B, the equivalent output-referred current noise is

$$i(t) = -G_{mo}v_n(t) \tag{35}$$

where G_{mo} is the equivalent transconductance from the ground noise source to the differential output of the buffer, calculated in Appendix B.

Now we can use the time-domain jitter model in case of deterministic signals, expressed by (10), to find jitter of the buffer. It is easy to see that, since the ISF of the circuit, defined in (6), is the largest at the nominal crossing time, the maximum crossing time variation occurs when the ground noise pulse (34) ends right at the nominal crossing time. In other words, the worst-case jitter will occur when the start time of the noise pulse is $t_0 = 0$. With this in mind, and combining (35) and (34) with (10), maximum jitter is

$$|t_j|_{\max} = \frac{RC}{2I}G_{mo}V_n. \tag{36}$$

Substituting the values for R, C and I from Table II, assuming that $V_n = 5$ mV and with the transconductance found in Appendix B, $G_{mo} = 3$ mA/V, estimated maximum jitter is

$$|t_j|_{\max} = 714 \text{ fs}. \tag{37}$$

This result is compared to the result of exhaustive transient simulation in HSPICE. In the simulations, arrival time of the 5-mV ground voltage pulse was varied, while keeping its duration at t_x, and variations of the buffer output crossing time were recorded. As expected, the maximum crossing time variation occurred when arrival time of the ground noise pulse was $t_0 = 0$ which yielded the maximum jitter:

$$|t_{j,\text{HSPICE}}|_{\max} = 600 \text{ fs}. \tag{38}$$

When the predicted jitter (37) is compared to the simulated jitter (38), the error introduced by our model is calculated to be 18.8%, which seems quite significant. However, further analysis shows that most of this error is due to the use of the overly simplified method for finding the transconductance from the ground noise source to the output of the buffer. In the analysis presented in Appendix B, we used a low-frequency small-signal model of the CML buffer, which neglects numerous secondary parameters of the circuit (e.g., gate-source and other parasitic capacitances, substrate and gate resistances, etc.). Performing the AC analysis in HSPICE, it turns out that, instead of the constant value G_{mo}, the transconductance can be expressed more precisely as a single-pole function

$$G_m(jf) = \frac{G_{mo}}{1 + j\frac{f}{f_G}} \tag{39}$$

where f_G is the cutoff frequency caused by the parasitics, and is about 25 GHz. (Expression (39) for the transconductance can also easily be found analytically, if we know the values of the parasitics in the CML buffer circuit: pole f_G is caused by the equivalent parasitic capacitance at the drain of the tail current source transistor m_1 in Fig. 8.) Now we can use this more accurate expression for the transconductance together with our frequency-domain jitter model, to find the Fourier transform of the crossing time variation, $T_j(jf)$. According to (19)

$$\begin{aligned} T_j(jf) &= H_j(jf, t_x)I(jf) \\ &= -H_j(jf, t_x)G_m(jf)V_n(jf) \end{aligned} \tag{40}$$

where $H_j(jf, t_x)$ is the noise-to-jitter system function given by (18), and $V_n(jf)$ is the Fourier transform of the noise pulse $v_n(t)$ from (34). [The expression for $V_n(jf)$ is given in Appendix C.] Calculating $T_j(jf)$ and then its inverse Fourier transform at the nominal crossing time, $t_j(t_x)$, it can be shown that the maximum jitter of the buffer is now

$$|t_j|_{\max} = 581 \text{ fs} \tag{41}$$

which is much closer to the simulated value given in (38). The error introduced by our method for predicting jitter is now only 3.4%.

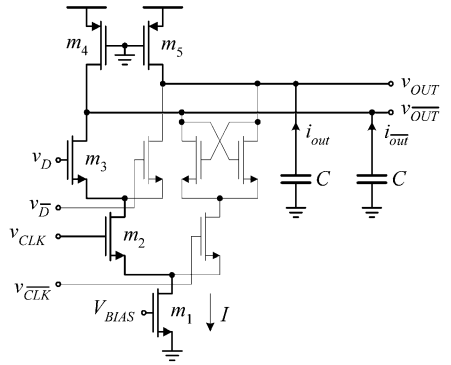

Fig. 9. Schematic of the CML latch.

At this point, an interesting practical observation can be made. If we compare deterministic jitter found in this example, with the random jitter caused by device noise found in the previous example, we can see that, even though the amplitude of the ground noise pulse is only 5 mV, the jitter that it causes is significantly larger than the random jitter. Therefore, when a very low-jitter performance is required, the greatest amount of design effort needs to be devoted to minimizing deterministic disturbances, such as power supply noise, and their effects on jitter.

V. Conclusion

In this paper, we present an analysis of jitter due to random and deterministic noise in nonautonomous (driven) MOS current-mode logic (CML) circuits. For this purpose, a method that explains the transformation of noise into jitter is derived. Jitter generation is modeled as a linear time-variant process, characterized with its impulse response function in the time domain, and a system function in the frequency domain. These characteristic functions are derived based on the impulse sensitivity function, ISF, which is calculated analytically and expressed in terms of circuit parameters. The method yields closed-form expressions which relate jitter to circuit and noise parameters. We use these expressions to estimate jitter in two different CML circuits, with different sources of noise. In the first example, we examine jitter due to random device noise in a CML frequency divider. We show that most of the jitter originates from the thermal noise of the tail current source transistor and pMOS load devices, while a smaller amount of jitter is due to $1/f$ (flicker) noise. In the second example, we study jitter of a CML buffer, caused by deterministic ground noise. Our analysis shows that even small variations of the ground voltage can cause jitter, which is significantly larger than the jitter caused by random device noise. This conclusion illustrates the importance of suppressing deterministic noise sources for low-jitter performance. In both examples, jitter estimates are compared against results obtained via exhaustive HSPICE simulation. The comparison shows that the estimated jitter matches the simulated jitter with an error of up to 3.4%.

Appendix A
Calculation of the Output-Referred Device Noise of the CML Frequency Divider

As mentioned earlier, jitter of the frequency divider will be caused only by the device noise originating from the slave latch [13]. Schematic of a CML latch is given in Fig. 9.

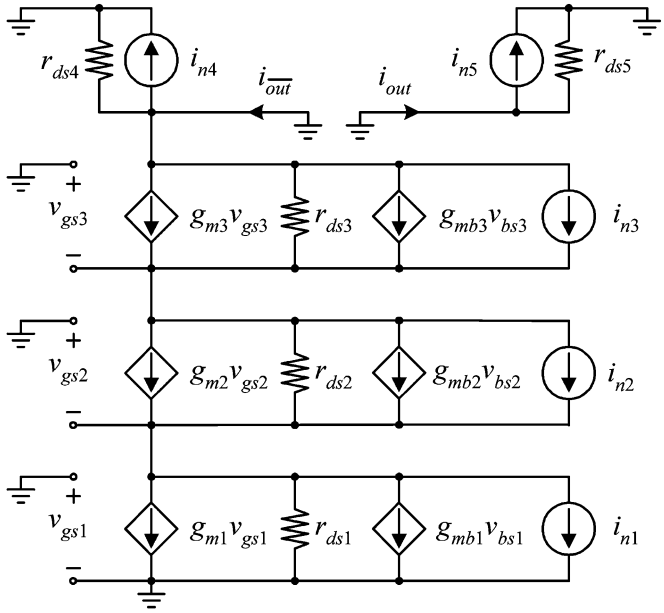

Fig. 10. Small-signal schematic of the CML latch from Fig. 9 after the arrival of the clock signal, with $v_D =$ '1' and $v_{\overline{D}} =$ '0'. i_{n1}–i_{n5} are the device noise sources associated with transistors m_1–m_5, respectively.

Let us observe the latch right after the arrival of the clock signal, i.e., when v_{CLK} is switching from logical '0' to logical '1' and $v_{\overline{\mathrm{CLK}}}$ is switching from '1' to '0'. According to the assumption introduced in Section II, switching is instantaneous and the entire current of transistor m_1, which acts as a biasing current source, is immediately switched through transistor m_2. Let the logic levels of the data inputs be $v_D =$ '1' and $v_{\overline{D}} =$ '0', and the levels of the outputs before the arrival of the clock be $v_{\mathrm{OUT}} =$ '0' and $v_{\overline{\mathrm{OUT}}} =$ '1'. According to these assumptions, after the arrival of the clock, capacitor at output OUT will start charging through transistor m_5, while the capacitance at $\overline{\mathrm{OUT}}$ will start discharging through transistors m_1–m_3.

The equivalent small-signal schematic of the latch is shown in Fig. 10. In order to simplify the hand-analysis, we are using the low-frequency models of transistors, which is acceptable since the output load capacitance is the dominant one. Fig. 10 also shows device noise sources i_{n1}–i_{n5}, associated with transistors m_1–m_5, respectively. i_{out} and $i_{\overline{\mathrm{out}}}$ are the equivalent output-referred noise currents that we are trying to compute.

The first step toward finding the output-referred noise currents is to find current gains β_1–β_4 from transistors m_1–m_4 to output $\overline{\mathrm{OUT}}$, as well as the current gain β_5 from m_5 to OUT:

$$\beta_l = \left.\frac{i_{\overline{\mathrm{out}}}}{i_{nl}}\right|_{i_{\mathrm{nj}}=0,\forall j\neq l}, \text{ for } l = 1\ldots 4, \text{ and } \beta_5 = \frac{i_{\mathrm{out}}}{i_{n5}}.$$

Using the small-signal schematic of the latch, expressions for β_1–β_5 can be derived as shown in the equation at the bottom of the next page. In these expressions, $g_{ml\mathrm{eff}} = g_{ml} + g_{mbl}$ for $l = 2, 3$.

Using the values of the small-signal parameters summarized in Table III, current gains are found to be: $\beta_1 = 0.9, \beta_2 = 0.07$, $\beta_3 = 0.01, \beta_4 = 1$ and $\beta_5 = 1$. Finally, it should be noted that, when finding the small-signal parameters of the latch, its dc output voltages were kept at the values which they take at the nominal crossing time: $v_{\mathrm{OUT}} = v_{\overline{\mathrm{OUT}}} = V_{\mathrm{DD}} - IR/2$.

TABLE III
TRANSISTOR PARAMETERS USED IN CALCULATIONS OF THE OUTPUT-REFERRED NOISE OF THE CML LATCH

Devices	Parameters				
	I [μA]	g_m [mA/V]	g_{mb} [mA/V]	r_{ds} [kΩ]	K_f [pA]
m_1	315	2.8	/	4.4	4.2
m_2	315	2.2	0.3	2.8	21.5
m_3	315	1.8	0.2	3.0	21.5
m_4	157	/	/	1.2	323.7
m_5	157	/	/	1.2	323.7

The next step is to find PSDs of noise sources i_{n1}–i_{n5}. PSD of a MOSFET transistor in saturation is [22]

$$S_i(f) = \frac{K_f I^a}{f^b} + 4kT\left(\frac{2}{3}g_m\right)$$

and this expression will be used for transistors m_1–m_3. PSD of a MOS transistor in the linear region is

$$S_i(f) = \frac{K_f I^a}{f^b} + 4kT\frac{1}{r_{ds}}$$

and this expression will be used for finding noise of transistors m_4 and m_5. In the formulas above, k is the Boltzmann constant, T is the absolute temperature, a and b are process-dependent parameters close to one. K_f is the flicker noise coefficient and it is a function of the process parameters and transistor dimensions. Values K_f of transistors m_1–m_5 are given in Table III. Note that flicker noise does not depend on the region of operation, as confirmed in [23].

Finally, we can calculate PSDs of the total output-referred device noise of the CML latch:

$$S_{\overline{\text{out}}}(f) = \sum_{l=1}^{3}\beta_l^2\left\{\frac{K_{fl}I_l^a}{f^b} + 4kT\left(\frac{2}{3}g_{ml}\right)\right\}$$

and

$$S_{\text{out}}(f) = \beta_5^2\left\{\frac{K_{f5}I_5^a}{f^b} + 4kT\frac{1}{r_{ds5}}\right\}.$$

Using the values for current gains β that we found earlier, and parameters from Table III, the PSDs are

$$S_{\overline{\text{out}}}(f) = \frac{K_F}{f} + K_W = \frac{2.6\times10^{-15}A^2}{f} + 4.1\times10^{-23}\,\text{A}^2/\text{Hz}$$

and

$$S_{\text{out}}(f) = \frac{K_F}{f} + K_W = \frac{1.9\times10^{-15}A^2}{f} + 1.4\times10^{-23}\,\text{A}^2/\text{Hz}.$$

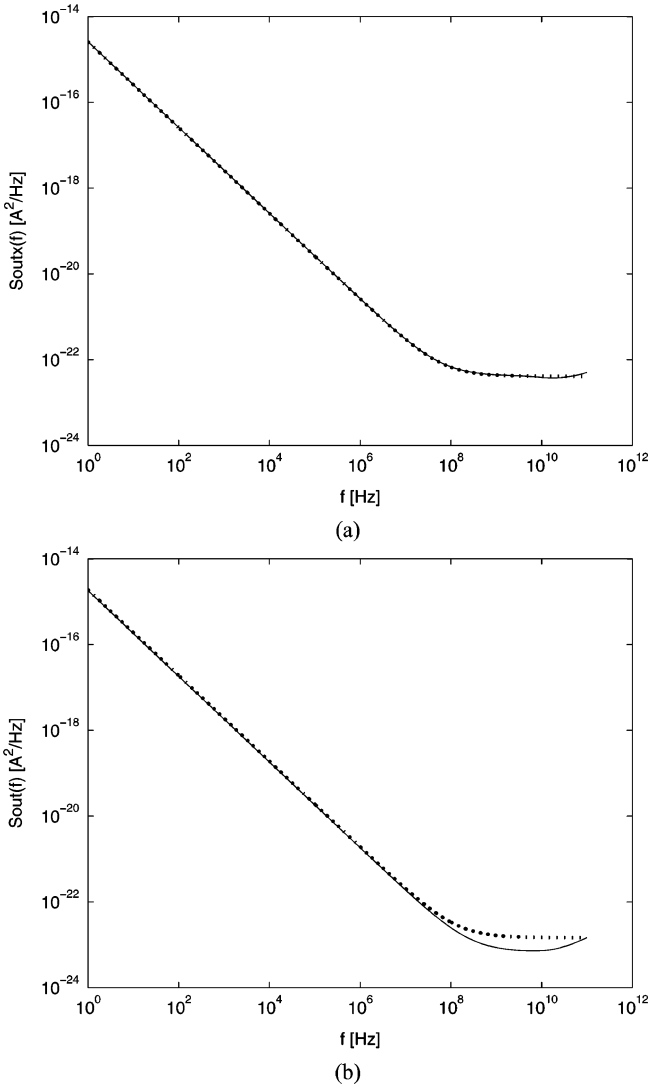

Fig. 11. (a) Comparison of the calculated and simulated PSD $S_{\overline{\text{out}}}(f)$, and (b) Comparison of the calculated and simulated PSD $S_{\text{out}}(f)$.

$$\beta_1 = \frac{g_{m2\text{eff}}r_{ds1} + \frac{r_{ds1}}{r_{ds2}}}{1 + g_{m2\text{eff}}r_{ds1} + \frac{r_{ds1}}{r_{ds2}} + \frac{1}{g_{m3\text{eff}}r_{ds2} - \frac{r_{ds2}}{r_{ds3}}}}$$

$$\beta_2 = \frac{1}{1 + g_{m2\text{eff}}r_{ds1} + \frac{r_{ds1}}{r_{ds2}} + \frac{1}{g_{m3\text{eff}}r_{ds2} - \frac{r_{ds2}}{r_{ds3}}}}$$

$$\beta_3 = \frac{1}{1 + g_{m3\text{eff}}r_{ds2} + g_{m3\text{eff}}g_{m2\text{eff}}r_{ds1}r_{ds2} + g_{m3\text{eff}}r_{ds1} - \frac{r_{ds2}}{r_{ds3}} - \frac{g_{m2\text{eff}}r_{ds1}r_{ds2}}{r_{ds3}} - \frac{r_{ds1}}{r_{ds3}}}$$

$$\beta_4 = 1, \quad \beta_5 = 1.$$

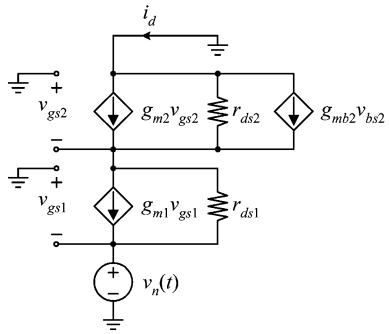

Fig. 12. Small-signal model of the buffer circuit after the switching.

Coefficients K_F and K_W found above were used in (28) and (31), respectively, for the frequency divider jitter calculations.

Lastly, we should mention that equivalent noise sources at the two outputs are mutually uncorrelated, which should be obvious from the small-signal model of the latch shown in Fig. 10, since transistor m_5 is disconnected from the rest of the circuit.

To verify the above calculations, noise analysis of the CML latch was performed in HSPICE and simulation results were compared to the calculated PSDs. Fig. 11(a) shows the simulated (solid line) and the calculated (dotted line) PSD $S_{\overline{\text{out}}}(f)$, while Fig. 11(b) shows the simulated (solid line) and the calculated (dotted line) PSD $S_{\text{out}}(f)$.

APPENDIX B
CALCULATION OF THE EQUIVALENT GROUND-TO-OUTPUT TRANSCONDUCTANCE OF THE CML BUFFER CIRCUIT

Observe the CML buffer circuit from Fig. 8 when v_{in} is switching from logical '0' to logical '1'. The switching is instantaneous, and the biasing current I is immediately steered through transistor m_2 which discharges the capacitance at output $\overline{\text{OUT}}$. The small-signal schematic of the buffer after the switching is given in Fig. 12.

The noise current that affects the crossing time of the buffer outputs is the differential current $i_d = i_{\overline{\text{out}}} - i_{\text{out}}$. (In this case, the disturbance that causes jitter is a deterministic signal. Hence, instantaneous values of the noise currents at the two outputs add, rather than their variances.) To calculate i_d, we need to find the equivalent transconductance from $v_n(t)$ to the output. It should be noted that the ground noise also affects the crossing time by varying the resistances of the pMOS load transistors, but these effects at the two differential outputs cancel each other out. Therefore, the total i_d can be found from the circuit shown in Fig. 12. Also, we should mention that the substrates of all the nMOS transistors are tied to the same node (ground), and therefore, $v_{bs1} = 0$ and $v_{bs2} = v_n + v_{gs2}$.

Now it is easy to show that the transconductance is

$$G_{mo} = \frac{i_d}{v_n} = -\frac{g_{m1} + \frac{1}{r_{ds1}} + \frac{g_{mb2}}{(g_{m2}+g_{mb2})r_{ds1}+\frac{r_{ds1}}{r_{ds2}}}}{1 + (g_{m2} + g_{mb2})r_{ds1} + \frac{r_{ds1}}{r_{ds2}}}$$

Using the small-signal parameters found in HSPICE and summarized in Table IV, the transconductance is found to be $G_{mo} \approx g_{m1} = 3$ mA/V.

TABLE IV
SMALL-SIGNAL PARAMETERS OF THE LOW-FREQUENCY MODEL OF THE BUFFER CIRCUIT

Devices	Parameters		
	g_m [mA/V]	g_{mb} [mA/V]	r_{ds} [kΩ]
m_{n1}	3	/	8.3
m_{n2}	1.8	0.2	5.1

APPENDIX C
FOURIER TRANSFORM OF THE GROUND NOISE PULSE

Fourier transform of the ground noise pulse, $v_n(t)$, given by (34), is

$$V_n(jf) = t_x V_n \frac{\sin(\pi f t_x)}{\pi f t_x} e^{-j\pi f t_x}.$$

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