Dual-Edge Triggered Storage Elements and Clocking Strategy for Low-Power Systems

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***Abstract*—This paper describes the classification, detailed timing characterization, evaluation, and design of the dual-edge triggered storage elements (DETSE). The performance and power characterization of DETSE includes the effect of clocking at halved clock frequency and impact of load imposed by the storage element to the clock distribution network. The presented analysis estimates the timing penalty and power savings of a system based on DETSE, and gives design guidelines for high-performance and low-power application. In addition, the paper presents a class of dual-edge triggered flip-flops with clock load, delay, and internal power consumption comparable to the fastest single-edge triggered storage elements (SETSE). Our simulated results show that by halving the clock frequency, dual-edge clocking strategy can save about 50% of the power consumed by the clock distribution network, and relax the design of clock distribution system, while paying virtually no penalty in throughput.**

***Index Terms*—Clock distribution, dual-edge triggering, low power, storage elements.**

I. Introduction

INCREASING circuit speed is certain to remain the major goal in the future logic design evolution. Predictions in technology and performance scaling [1] indicate that the technology itself is not likely to provide required performance improvement, thus a portion of the performance is expected from circuit design innovations. More specifically, the timing overhead of the storage elements is supposed to decrease from today's roughly three fan-out-of-four delays (3 FO4) to about 1.5 FO4. In addition, innovations in clocking subsystem are needed to reduce its power consumption relative to the total power. The break-up of high-performance processor power consumption shows about 30%–50% power spent for clocking only, in high-performance processors, [2], [3]. These innovations are particularly important as the power consumption of high-end systems grows exponentially over time, with less and less efficient heat removal and no apparent technology solution in the near future.

Frequency scaling involves additional difficulties if the clock frequency continues to follow the trend predicted by the roadmap for the following years (3–5 GHz). With clock period reduced to 200 ps, the importance of clock uncertainties will increase, and complex multiple-phase clocking will become impractical due to increasingly large timing uncertainties and power consumption.

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In order to save on clocking power, dual-edge triggered (DET) clocking strategy uses DET storage elements (DETSE) that capture the value of the input after both rising and falling clock transitions. Otherwise, DETSE is nontransparent, i.e., it holds the captured value at the output. Thus, the DET clocking strategy provides a one-time solution to the frequency scaling by retaining the data throughput of single-edge triggered (SET) clocking at halved clock frequency. However, in order to fully exploit the power savings in the clock distribution network, this approach must ensure that the delay and energy consumption of DETSE must be comparable to those of SET storage elements (SETSE). Furthermore, use of both clock edges to synchronize the operation makes timing sensitive to clock duty cycle and increases clock uncertainties generated by the clock distribution system.

DET systems have been studied in the past decade [4]–[8]. However, the emphasis of virtually all previously published papers was on the circuit design of the storage elements. The consistent definition of timing and energy metrics was lacking, as well as an estimate of the effect that a dual-edge clocking has on a system power, which is a basis for a fair comparison between DET and SET strategies.

This paper is divided into seven sections. Section II gives the classification and timing characterization of DETSE. Section III discusses the effects of dual-edge clocking strategy on the design of the clock distribution system. Section IV reviews previously published DETSE. Section V presents new developed DETSE. Section VI shows the simulation results, and Section VII concludes the paper.

II. DETSE

DET clocking strategy uses DETSE that capture the value of the input after both low-to-high and high-to-low clock transitions. Otherwise, DETSE is nontransparent, i.e., it holds the captured value at the output [Fig. 1(a)]. A system that uses DETSE is shown in Fig. 2.

A DETSE can be classified as [9], [25] follows.

- Pulsed latch [Fig. 1(b)], which consists of a clock pulse generator and a transparent latch. The clock pulse generator creates a short pulse after both clock edges, which is then used as the clock input to the transparent latch;
- Flip-flop [Fig. 1(c)], which consists of the same building blocks as SET flip-flops. The pulse generator is active on both edges, or it combines the outputs of two pulse generators active at the opposite clock edges;
- Latch-MUX structure [LM, Fig. 1(d)], which consists of two latches, connected in parallel and transparent

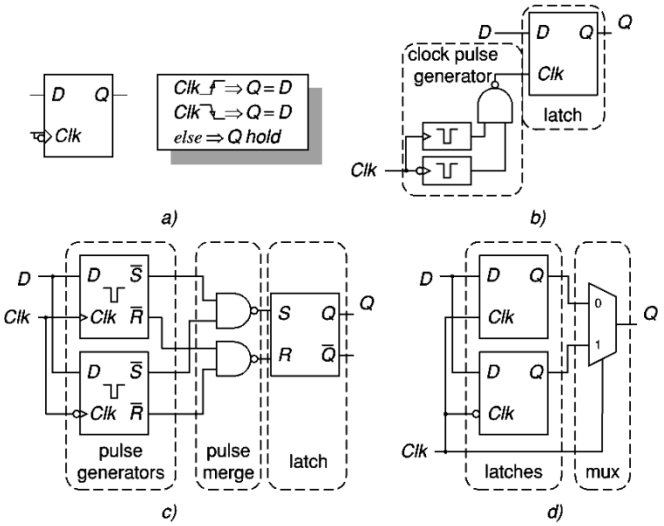

Fig. 1. Dual-edge-triggered storage elements. (a) Function. (b) Pulsed latch. (c) Flip-flop. (d) Latch-MUX.

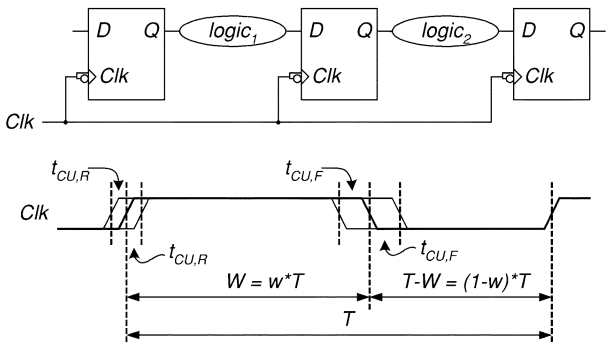

Fig. 2. System that uses DETSE and clock timing diagram.

on opposite levels of the clock, and a multiplexor that selects the output of the nontransparent latch at any time. Latch-MUX is a DET counterpart of the master-slave latch clocked with the complementary clock phases.

A. Timing Characterization

The timing in a system that uses DETSEs depends on the type of logic used and the number and mutual timing relationship between clock phases. In this section, we consider only systems that use single-phase clock and static logic. We use terms rising and falling clock edge, and indices R and F to distinguish between the two edges of the clock.

Following are the basic timing parameters of a DETSE, defined for each clock edge.

- Set-up time—maximum allowed data arrival with respect to the clock edge in order to correctly capture it;
- Hold time—minimum allowed data arrival after the clock edge in order to correctly capture the previous value;
- Propagation time (clock-to-output delay)—delay between the clock edge and the output switching to the new value.

Diagram of a system that uses DETSEs is shown in Fig. 2. Single-phase clock is specified by its period T, duty cycle (clock pulse width relative to period) w, clock pulse width W, which is equal to $w \cdot T$, and maximum clock uncertainty for rising and falling clock edge, $t_{\mathrm{CU},R}$ and $t_{\mathrm{CU},F}$, respectively. Setup time, hold time, and maximum and minimum clock-to-output delay are defined for both clock edges: $t_{\mathrm{SU}R}, t_{\mathrm{SU}F}, t_{\mathrm{HR}}, t_{\mathrm{HF}}, t_{\mathrm{CQ}R}, t_{\mathrm{CQ}F}, t_{\mathrm{cq}R}, t_{\mathrm{cq}F}$.

Note that when data is released at the rising edge of the clock, it is captured at the falling edge, and vice versa. Two requirements must be satisfied for each of the two clock edges, totaling four independent constraints. First, it must be assured that the data arrives to the receiving DETSE late enough to prevent its hold time violation. The correct operation must be assured even for the earliest arrival of the releasing clock edge, minimum clock-to-output and logic delay, and the latest arrival of the receiving clock edge. For the falling edge of the clock, the fast data must arrive to the receiving storage element at the earliest for hold time t_{HF} after the falling edge of the clock. Thus the following must be satisfied:

$$-t_{\mathrm{CU},F} + t_{\mathrm{cq}F} + t_l \geq t_{\mathrm{CU},F} + t_{\mathrm{HF}}. \tag{1}$$

Similarly, the data must reach receiving storage element at the earliest for hold time t_{HR} after its latest possible rising edge of the clock

$$-t_{\mathrm{CU},R} + t_{\mathrm{cq},R} + t_l \geq t_{\mathrm{CU},R} + t_{\mathrm{HR}}. \tag{2}$$

Equations (1) and (2) determine the minimum logic delay in the stage that prevents the hold time violation

$$t_l \geq \max((t_{\mathrm{HF}} + 2t_{\mathrm{CU},F} - t_{\mathrm{cq}F}), (t_{\mathrm{HR}} + 2t_{\mathrm{CU},R} - t_{\mathrm{cq}R})). \tag{3}$$

In addition to the above, the data released by the rising edge of the clock, and traversing logic block, must reach the receiving storage element at the latest for $t_{\mathrm{SU}F}$ prior to falling edge of the clock. This requirement must be satisfied even for most pessimistic storage element delay, logic delay and clock uncertainty

$$t_{\mathrm{CU},R} + t_{\mathrm{CQ},R} + t_L + t_{\mathrm{CU},F} + t_{\mathrm{SU}F} \leq w \cdot T. \tag{4}$$

Similarly, if the data is released at the falling edge and captured at the rising edge of the clock, the following relation holds:

$$t_{\mathrm{CU},F} + t_{\mathrm{CQ},F} + t_L + t_{\mathrm{CU},R} + t_{\mathrm{SU}R} \leq (1 - w) \cdot T. \tag{5}$$

Equations (4) and (5) determine the minimum clock period for given duty cycle

$$T \geq T_{\min} = \max\left(\frac{t_{\mathrm{CU},R} + t_{\mathrm{CQ}R} + t_L + t_{\mathrm{SU}F} + t_{\mathrm{CU},F}}{w}, \frac{t_{\mathrm{CU},F} + t_{\mathrm{CQ}F} + t_L + t_{\mathrm{SU}R} + t_{\mathrm{CU},R}}{1-w} \right). \tag{6}$$

Alternatively, if the clock period T is specified, the above analysis provides the maximum allowable logic delay

$$t_L \leq \min\left(\begin{array}{c} w \cdot T - (t_{\mathrm{CQ}R} + t_{\mathrm{SU}F}), \\ (1-w) \cdot T - (t_{\mathrm{CQ}F} + t_{\mathrm{SU}R}) \end{array} \right) - t_{\mathrm{CU},R} - t_{\mathrm{CU},F}. \tag{7}$$

It is not always possible to control the clock duty cycle. Therefore, an important special case for practical purpose is

symmetric clock ($w = 0.5$). In case of $w = 0.5$, (6) and (7) become

$$T \geq T_{\min} = 2 \cdot \begin{pmatrix} \max(t_{CQR} + t_{SUF}, t_{CQF} + t_{SUR}) \\ + t_L + t_{CU,R} + t_{CU,F} \end{pmatrix} \quad (8)$$

$$t_L \leq T/2 - \max \begin{pmatrix} t_{CQR} + t_{SUF}, \\ t_{CQF} + t_{SUR} \end{pmatrix} - t_{SU,R} - t_{CU,F}. \quad (9)$$

In general, the optimum point is obtained by finding the clock duty cycle w_{opt} that minimizes T while both (4) and (5) are satisfied

$$w_{\text{opt}} = \frac{1}{1 + \dfrac{t_{CQF} + t_{SUR} + t_L + t_{CU,R} + t_{CU,F}}{t_{CQR} + t_{SUF} + t_L + t_{CU,R} + 2t_{CU,F}}}. \quad (10)$$

Corresponding minimum achievable clock period is

$$T_{\min} = t_{CQR} + t_{CQF} + t_{SUR} + t_{SUF} + 2t_L + 2t_{CU,R} + 2t_{CU,F}. \quad (11)$$

If the clock period T is specified and the goal is to find maximum logic delay, (10) and (11) become (12) and (13)

$$w_{\text{opt}} = \frac{1}{2}\left(\frac{t_{CQR} - t_{CQF} + t_{SUF} - t_{SUR}}{T} + 1\right). \quad (12)$$

Corresponding maximum logic delay is defined by (13)

$$t_L \leq \frac{1}{2}(T - (t_{CQR} + t_{CQF} + t_{SUR} + t_{SUF})) - t_{CU,R} - t_{CU,F}. \quad (13)$$

The above analysis shows that in general case clock must be asymmetric ($w \neq 0.5$) for optimal operation. The measure of this asymmetry is the difference between the overheads of the storage element in two half-periods of the clock, (10) and (12). Since the optimum duty cycle does not depend on the logic delay, it is same for all paths if the same DETSE is used throughout the system.

Equations (10) and (12) also indicate how to achieve the optimum operation with arbitrary clock duty cycle. For example, the condition for $w_{\text{opt}} = 0.5$ leads to

$$t_{CQR} + t_{SUF} = t_{CQF} + t_{SUR}. \quad (14)$$

Thus, a requirement for a good design of a DETSE with symmetric clock is to closely comply with (14). In order to obtain most performance, it is necessary to minimize both sides of (14).

Note that, while the above analysis is useful for understanding the design issues, in many practical cases, a nonsymmetrical clock is not feasible due to the limitations of the clock generator and clock distribution. In Section VI, we will show that the sensitivity of a DETSE to the duty cycle variation is small enough to avoid any significant performance degradation even with the symmetrical clock.

B. Timing Parameters and Metrics

One must define the timing metrics of a storage element in order to be able to quantitatively express and optimize its performance, and to compare it to other storage elements and strategies. The appropriate timing metrics is one that reflects the time that the clocking strategy leaves available to the useful logic computation. Thus the timing metrics is closely related to the clocking strategy, and not only to the storage element itself.

Most common approaches define timing parameters of a storage element based on the *signal integrity criteria*. For example, setup time and hold time are defined as the points where some critical internal node experiences (unwanted) glitch of defined magnitude—e.g., 10% VDD, 0.2 V, etc. This approach binds the definition to a design-specific node, which disallows a fair comparison of different storage elements. In addition, the definition is imprecise—defined threshold may be far noncritical for some storage elements, while it may cause severe internal signal degradation for others. Other approaches define setup and hold times at points where the clock-to-output characteristic experiences the degradation equal to some defined percentage of the nominal clock-to-output delay. Compared to the above definition based on a glitch, this definition is universal, and thus better to some extent. However, it is unfair as it relates the definition to the nominal clock-to-output time, so that different degradations are allowed for the designs with different nominal delays. In addition, the specification of delay degradation percentage is vague. As an alternative to these signal integrity criteria, the remainder of this section presents the *performance-based* definitions of setup and hold times of a DETSE.

As it is illustrated by the above discussion, the "delay" of a DETSE is not related to a physical delay parameter such as data-to-output delay, as is the case with SETSE [10], [25]. In order to relate the timing metrics to physical delay parameters, we define the timing overhead of a DETSE as the time that the DET clocking strategy takes from the clock cycle, thus indicating the time left to the logic for the useful computation. The timing overhead of DET clocking strategy can be directly seen in (4)–(14). It depends on whether the data is released at the rising or falling clock edge. In addition, the timing overhead is a function of the timing parameters of storage element, clock period T, duty cycle w, and clock uncertainties $t_{CU,R}$ and $t_{CU,F}$, (7). Since the clock uncertainty is a system parameter, and not the parameter of the storage element, we do not include it in the timing overhead of the storage element. Accordingly, the timing overhead of a DETSE can be obtained from (7)

$$t_D = T/2 - t_{L,\max} = \max \begin{pmatrix} T \cdot (0.5 - w) + t_{CQR} + t_{SUF} \\ T \cdot (w - 0.5) + t_{CQF} + t_{SUR} \end{pmatrix}. \quad (15)$$

In the important special case when the clock is symmetric ($w = 0.5$), this timing overhead becomes

$$t_D = \max(t_{CQR} + t_{SUF}, t_{CQF} + t_{SUR}). \quad (16)$$

In another important special case when the clock duty cycle w is optimally chosen according to (12), timing overhead is obtained from (15)

$$t_D = \frac{t_{\mathrm{CQ}R} + t_{\mathrm{CQ}F} + t_{\mathrm{SU}R} + t_{\mathrm{SU}F}}{2}. \tag{17}$$

Equations (15)–(17) provide the consistent performance-based method for defining setup and hold time of DETSEs. In this course, we observe the clock-to-output characteristics of a DETSE. There exist two characteristics, one corresponding to the rising edge of the clock and the other corresponding to the falling edge of the clock. In general, the rising-edge and falling-edge clock-to-output characteristics are not equal. These characteristics have similar shape as the clock-to-output characteristic of a SETSE, described in [25], [10].

Setup Time: According to the performance-based criteria, the setup times of a DETSE are defined as data-to-clock delays on rising-edge and falling-edge clock-to-output characteristics that result in the minimum timing overhead, (15)–(17). In general case, described by (15), this definition depends on system-level parameters clock period T and duty cycle w. We will discuss only two special cases: 1) when duty cycle $w = 0.5$ (symmetric clock) and 2) when duty cycle is optimal in terms of (12). For these two special cases, setup times $t_{\mathrm{SU}R}$ and $t_{\mathrm{SU}F}$ can be found as the values of data-to-rising-clock and data-to-falling-clock times, $t_{D-\mathrm{Clk},R}$ and $t_{D-\mathrm{Clk},F}$, that minimize (16), (17) regardless of the clock period T. We are allowed to push the data arrival of a DETSE as far as its clock-to-output time is not degraded enough (due to this late data arrival) to violate the timing of the consequent pipeline stage. In this way, the timing overhead t_D is a function of two independent variables, $t_{D-\mathrm{Clk},R}$ and $t_{D-\mathrm{Clk},F}$, since clock-to-output delays are direct functions of the data-to-clock delays.

In the case when $w = 0.5$, (16) needs to be minimized. Using simple calculus, it can be shown that the data-to-clock delays that yield minimum timing overhead must satisfy the following:

$$\frac{\partial t_{\mathrm{CQ}R}}{\partial t_{\mathrm{SU}R}} \cdot \frac{\partial t_{\mathrm{CQ}F}}{\partial t_{\mathrm{SU}F}} = 1 \tag{18}$$

$$t_{\mathrm{CQ}R} + t_{\mathrm{SU}F} = t_{\mathrm{CQ}F} + t_{\mathrm{SU}R}. \tag{19}$$

Equation (18) states that the slopes of the two clock-to-output characteristics are mutually reciprocal at the point of minimum timing overhead. Equation (19) states that the timing overheads in two half-cycles must be equal. Fig. 3 represents an example of the timing overhead t_D of the DETSE for $w = 0.5$, as a function of rising-edge and falling-edge data-to-output delays.

From the above analysis, the timing parameters of a DETSE should be set so that the cross-sums $t_{\mathrm{SU}R} + t_{\mathrm{CQ}F}$ and $t_{\mathrm{SU}F} + t_{\mathrm{CQ}R}$ are minimized. More specifically, if the falling-edge capture fails for smaller data-to-clock delay than the rising-edge capture, it is more important to optimize falling-edge than rising-edge clock-to-output time and vice versa.

Equations (18) and (19) determine the lower bound of the timing overhead of the DET clocking strategy. If there exists a significant asymmetry between rising-edge and falling-edge clock-to-output characteristics, this minimum may be positioned at the point with a large slope of one of the clock-to-output characteristics. As a result, reliability of the DETSE may be compromised, since the large slope of the characteristic usually means that the operating point is very close to the failure region. In such cases, a maximum acceptable slope of the clock-to-output characteristic should be specified from the point of signal integrity and reliability, and the optimum point found in the allowed area. The optimum point obtained in this way is slightly sub-optimal, but this degradation is negligible in most practical cases.

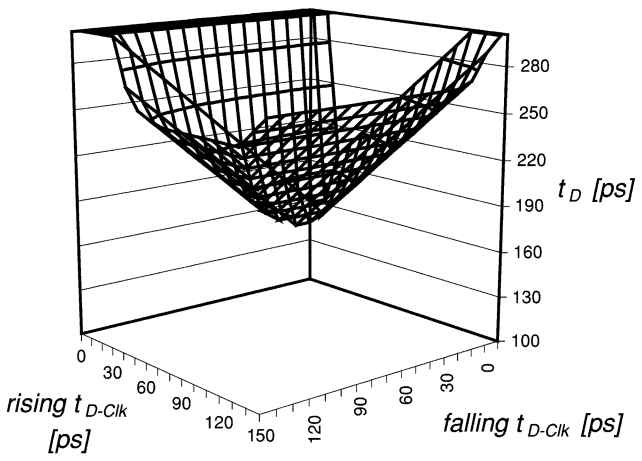

Fig. 3. Timing overhead of DET storage element for symmetric clock as a function of D-Clk delays.

In case when the clock duty cycle w is optimal in terms of (12), (17) must be minimized. This requirement yields the same result as in the case of SET flip-flop [11], [25]

$$\frac{\partial t_{\mathrm{CQ}R}}{\partial t_{\mathrm{SU}R}} = \frac{\partial t_{\mathrm{CQ}F}}{\partial t_{\mathrm{SU}F}} = -1. \tag{20}$$

Thus, if we are able to operate with optimal clock duty cycle, the optimal setup time for both rising and falling edge of the clock is the one that also minimizes data-to-output delay through the storage element.

Hold Time: Hold time of a DETSE must be defined so that the clock-to-output delay for all allowed data arrivals after the hold time is not greater than maximum clock-to-output delay on the setup side of the same characteristic, for both edges of the clock [11]. Internal race immunity (IRI) is the difference between minimum clock-to-output delay and maximum hold time [12]. It is the fast path safety margin of the pipeline stage with same releasing and receiving storage element, without logic between storage elements and without clock uncertainties. For the safe operation without logic between storage elements, the IRI must be higher than the maximum clock uncertainty. IRI of a DETSE is worse of internal race immunities for falling and rising edges of the clock

$$\mathrm{IRI} = \min(t_{\mathrm{cq}R} - t_{\mathrm{HR}}, t_{\mathrm{cq}F} - t_{\mathrm{HF}}). \tag{21}$$

III. System-Related Issues of DET Clocking

As shown in Section II-A, a DETSE yields maximum performance if it operates with the optimal clock duty cycle. However, this assumption poses a difficult requirement to the system, and

it may require too complex clock distribution network. Our goal is to estimate the performance of DETSE assuming the same clock distribution as in single-edge systems. For this reason, we assume fixed clock duty cycle of 50%, thus taking into account the performance degradation if this duty cycle is nonoptimal. For the optimization and the performance evaluation of DETSE, the timing metric is used that corresponds to the time taken from the clock half-cycle, assuming 50% clock duty cycle, given by (16).

Use of dual-edge clocking has a large impact on power and performance of a system. First, distributing clock with halved frequency of a SET system saves a considerable clock power, which is discussed in Section III-A. Second, using the clock with halved frequency relaxes the requirement on the clock distribution system, resulting in "cleaner" signal when the clock frequency is comparable to the bandwidth of the distribution system. However, use of both clock edges to synchronize the operation makes timing sensitive to clock duty cycle and increases clock uncertainties generated by the clock distribution system. This impact of performance of clock distribution system on dual-edge clocking is described in Section III-B.

A. Energy Savings in Clock Distribution System

This section analyzes power savings in the DET clock distribution system due to clocking at half the clock frequency of a SET system. In order to estimate the potential power saving in the clock distribution system, we model the effect of the storage element to the clock distribution by its clock load. The internal power of the storage elements is excluded from the analysis to simplify the derivation, and it must be added to the power of the clock distribution to obtain total clock-related power. In addition, in Section VI we show that the DETSE can indeed be designed with internal power and timing overhead comparable to the representative SETSEs, enabling us to roughly restrict the overall effect of the dual-edge clocking to the benefit of the energy savings of the clock distribution system.

A crucial parameter in determining potential advantage of DETSE is the total switching load in the clock distribution network (due to storage elements, clock buffers and wires) for SET and DET system. We find this load on the example of a H-tree clock distribution network with L levels in a microprocessor die of size $s \times s$ with M storage elements, Fig. 4(a). Each driver in the level L supplies clock to an area of dimensions $s/2^{L-1}$ by $s/2^{L-1}$ (local domain) that contains $M/4^{L-1}$ storage elements. In the local domain, the clock is distributed using individual wires from the central spine to the storage element, as shown in Fig. 4(a). Parameters c_w and $C_{\rm Clk}$ designate wire capacitance per unit length and clock load of a single storage element, respectively. We neglect wire resistance, so that the width, and thus capacitance, of the wires do not depend on the clock load of the storage elements.

Under the above assumptions, it can be shown that the total load in the H-tree, including clock load of storage elements is

$$C_H = \frac{4^L-1}{3\cdot 4^{L-1}} M\cdot C_{\rm Clk} + c_w s\cdot\left[\frac{M}{3\cdot 2^{L-1}}\cdot\left(\frac{4^L-1}{4^L}\right)+\frac{5\cdot 4^{L-1}+1}{3\cdot 2^{L-2}}-3\right]. \quad (22)$$

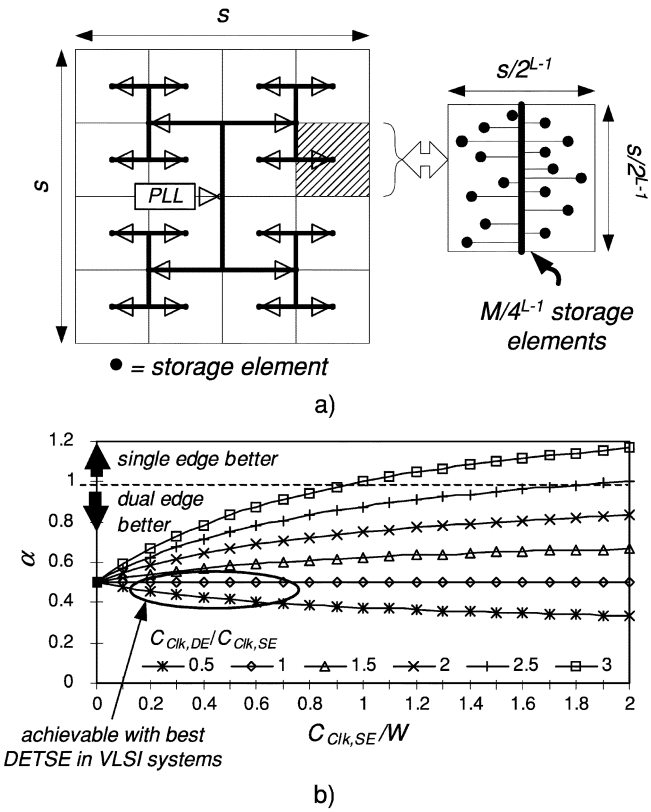

Fig. 4. Clock distribution: (a) H-tree clock distribution network and (b) H-tree power consumption comparison between dual-edge and single edge systems.

The derivation of (22) is given in the Appendix. The first item in the right-hand side of (22), is the portion of the H-tree capacitance that depends on the clock load of a storage element

$$C_{\rm Clk,tot} = \frac{4^L-1}{3\cdot 4^{L-1}} M\cdot C_{\rm Clk}. \quad (23)$$

If $4^L \gg 1, C_{\rm Clk,tot}$ can be approximated as $4M\cdot C_{\rm Clk}/3$. The remainder of the right-hand side of (22) represents the wire load and the load of the buffers needed to drive these wires

$$C_{\rm WIRE} = c_w s\cdot\left[\frac{M}{3\cdot 2^{L-1}}\cdot\left(\frac{4^L-1}{4^L}\right)+\frac{5\cdot 4^{L-1}+1}{3\cdot 2^{L-2}}-3\right]. \quad (24)$$

The parameter $C_{\rm WIRE}$ is the part of the clock distribution load that is independent of the clock load of the storage element. If $M \gg 4^L \gg 1, C_{\rm WIRE} \approx c_w\cdot s\cdot M/(3*2^{L-1})$.

To estimate the power savings of DET clocking, we form the coefficient α, which is the ratio of the clock distribution switching power consumptions of DET and SET systems. Using the above approximations of (23) and (24), we obtain

$$\alpha = \frac{P_{\rm DE}}{P_{\rm SE}} = \frac{1}{2}\cdot\frac{(C_{\rm WIRE}+C_{\rm Clk,tot,DE})}{(C_{\rm WIRE}+C_{\rm Clk,tot,SE})} = \frac{1}{2}\frac{(1+C_{\rm Clk,DE}/W)}{(1+C_{\rm Clk,SE}/W)}. \quad (25)$$

In (25), $W = c_w\cdot s/2^{L+1}$ is the average capacitance of the wire needed to route the clock signal from the level L buffer to a storage element, and indices DE and SE correspond to dual edge and single edge clocking, respectively. The ratio $C_{\rm Clk}/W$

is the measure of the transistor versus wire load that a storage element contributes to the local clock driver. This ratio depends on the topology of the storage element, size of the local clock domain, and the ratio of unit wire capacitance versus unit transistor capacitance in a given technology.

Fig. 4(b) presents the switching power ratio α versus $C_{\mathrm{Clk,SE}}/W$ for the above example of H-tree, for various ratios of clock loads of DETSE and SETSEs, calculated using (25). Note that in a typical modern custom design in today's technologies, $C_{\mathrm{WIRE}}(W)$ is usually greater than $C_{\mathrm{Clk,tot}}(C_{\mathrm{Clk}})$, so that the ratio C_{Clk}/W is smaller than 1. Equation (25) and Fig. 4(b) state that a DET system saves about 50% of clock distribution power either when the switching capacitance of the clock distribution system is dominated by the wire load, or when the clock load of a DETSE is comparable to that of a SETSE. Note that in many high-performance clock distribution systems, wire load is even more pronounced than in the H-tree (e.g., clock grid, or wide shielded clock wires routed on higher metal layers), so that the saving that can be achieved by using dual-edge clocking strategy may be even higher.

The effect of the dual-edge clocking to the overall system's power is a complex function of number of the storage elements on die, die size, type of the clock distribution system, technology parameters such as the ratio of unit wire capacitance to the unit gate capacitance, in addition to the design of the storage element itself. Therefore, it is not possible evaluate exact system power savings available to the dual-edge clocking without the knowledge of the entire system. In general, $C_{\mathrm{Clk,SE}}/W$ is typically close to or smaller than 1 in a modern custom VLSI system, and DETSE can be designed with clock load comparable to or even smaller than that of representative SETSE, resulting in achievable power savings in clock distribution system of about 50% or slightly more, as indicated in Fig. 4(b). To further illustrate the power-saving potential of the DET system to the system power consumption, the reader is referred to [13], which presents a simulation of LeonSPARC core, synthesized with one of the best commonly used SETSEs—C^2MOS master-slave latch [14], and with DET symmetric pulse generator flip-flop (SPGFF, see Section V-B), using a H-tree with five levels of clock buffers. The replacement of the SET C^2MOS with DET SPGFF resulted in clock distribution power savings of 51.9%, and total power saving of 17.9%.

B. Impact of Nonidealities in Clock Distribution System on Dual-Edge Clocking

As shown in (7), the clock duty cycle affects the portion of the clock half-cycle available to the logic computation. Therefore, control of this clock duty cycle is a major concern in DET systems. Typical specifications of the clock that allow large variation of the clock duty cycle (e.g., 45%–55%) are not acceptable in DET clocking strategy. Instead, the uncertainty of the clock width must be reduced to the same order as the uncertainty of the clock period. A method for clock generation and distribution that controls the clock duty cycle to $50\% \pm 0.5\%$ at the clock frequency of 433 MHz is presented in [15].

Another effect of clock distribution system to the dual-edge clocking is the clock width distortion due to the difference between the pull-up and pull-down driving strengths of the clock buffers. This distortion is caused by unbalanced process parameters for pMOS and nMOS transistors. In effect, the delay between rising edge of the clock at the releasing DETSE and falling edge of the clock at the receiving DETSE may be slightly different than duty cycle of the master clock at the clock generator. Since this delay difference varies from one DETSE pair to another, it can be seen as clock uncertainty generated by the clock distribution system. Note that this clock uncertainty may exist even if the same buffers are used to transfer the consecutive rising and falling edge of the clock, i.e., if the releasing and receiving DETSE are in the same local clock domain.

Typically, one branch of the clock distribution is included in the feedback loop of the clock generator [15] to ensure that the output of the clock distribution (clock in local domain), and not the output of the clock generator (usually a PLL), is synchronous with the system clock. In combination with the circuit for the control of the clock width [15], this technique cancels the effect of the die-to-die variations to the clock distribution-induced uncertainty of the clock duty cycle. The impact of the within-die variations on this component of the clock duty cycle uncertainty still exists even in a balanced clock distribution network. Note, however, that no wire resistance or capacitance mismatch exists, and that only the difference between rising and falling delays along the same path in the clock distribution network due to mismatch in transistor drive strength accounts to this uncertainty.

IV. Review of DETSE

When the SET clocking strategy is replaced by the DET strategy, the performance of the DETSE must be comparable to the original SETSE in order to exploit the power savings due to halved clock frequency. In addition, as discussed in Section III-A, if the clock load of a DETSE is much larger than that of the SETSE, power savings due to the clock frequency reduction might be canceled by an increase in the switching capacitance. Therefore, the clock load is a crucial performance parameter of a DETSE. In this section, we give the review of the state-of-the-art DETSEs and examine their characteristics that affect the performance and energy consumption.

The storage elements are routinely required to provide a scanning mechanism for testing purposes, set/reset, or enable inputs. It is therefore important for any practical use of DETSEs to ensure that the implementation of this functionality is feasible with reasonable delay, power, and area overhead. The detailed discussion on implementing scan and set/reset capabilities to the DETSE is not addressed in this paper due to the space limitation. A reader interested in this subject is referred to [16], which gives some circuit solutions and shows that the overhead of the scan and set/reset function in DETSEs is comparable to that of the SETSEs.

A. Latch-MUX

1) Transmission-Gate Latch-MUX: The transmission-gate latch-MUX (TGLM) [4] Fig. 5(a), is dual-edge counterpart of the single-edge transmission-gate master-slave latch (SE-TGMS, [17]). The TGLM requires two complementary clock phases.

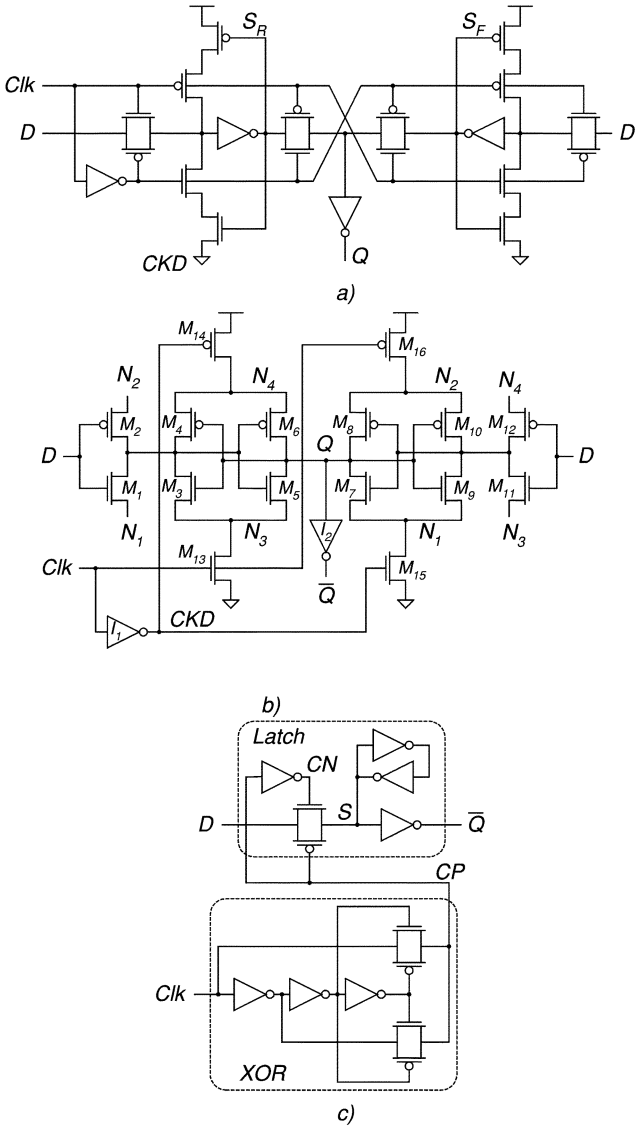

Fig. 5. State-of-the-art DETSE. (a) Transmission-gate latch-MUX. (b) C^{2}MOS latch-MUX. (c) Dual-edge transmission-gate pulsed latch (DE-TGPL).

The TGLM is the straightforward implementation of the latch-MUX structure [Fig. 1(d)] that uses transmission-gate (TG) latches. Therefore, principle of operation of the TGLM is described by operation of the latch-MUX structure, Section II, and the TG latch. Critical path of the TGLM consists of two TGs and two inverters. In addition, the switching activity of the critical nodes S_R and S_F directly depends on the input switching activity. The clock load of the TGLM is large, since each Clk and CKD drives twice as many large transistors compared to the TGMS latch. Thus, even though the TGLM offers good energy-delay tradeoff, large clock load may impair the benefits obtained by operation at reduced clock frequency.

2) C^{2}MOS Latch-MUX: The C^{2}MOS latch-MUX (C^{2}MOS LM) [5], Fig. 5(b), is dual-edge version of the C^{2}MOS master-slave latch [14]. The latch used in the C^{2}MOS LM is the conventional clocked CMOS latch. The multiplexor consists of two clocked CMOS inverters, high-Z-wired at the output, and a buffer inverter.

During the time when $\mathrm{Clk} = 0$, the forward path of the transparent latch M_1-M_2, the feedback path of the opaque latch M_9-M_{10}, and the path of the multiplexor M_7-M_8 are ON. Similarly, during the time when $\mathrm{Clk} = 1$, the forward path of the transparent latch M_{11}-M_{12}, the feedback path of the opaque latch M_3-M_4, and the path of the multiplexor M_5-M_6 are ON. The C^{2}MOS LM exploits this property of latch-MUX structure to share the clock transistors. In Fig. 5(b), only one pair of clocked transistors (M_{14}/M_{15} or M_{13}/M_{16}) is used for forward path of one latch, feedback path of the other latch, and multiplexor, at the same time. This transistor sharing greatly reduces clock load and power consumption, while not compromising the performance.

B. Pulsed Latches

1) Dual-Edge Transmission-Gate Pulsed Latch (DE-TGPL): [DE-TGPL, [6], Fig. 5(c)], is DET counterpart of the single-ended transmission-gate pulsed latch (TGPL, [6]). It consists of the clock pulse generator and the TG latch. The clock pulse generator creates a short pulse after each clock edge. During each pulse, the TG latch becomes transparent and captures the input data. At all other times, the latch is opaque and the change of the output is not allowed.

The pulse after each clock edge is obtained by performing the XOR/XNOR function of the input clock and the delayed clock. The delayed clock is obtained using an odd number of inverters. In this way, the clock and the delayed clock are at the same logic level only during the short time after both edges of the clock. In Fig. 5(c), the XOR pass-transistor logic gate is used to obtain a short negative pulse $(1 \rightarrow 0 \rightarrow 1)$ at the node CP, and a short positive pulse $(0 \rightarrow 1 \rightarrow 0)$ at the node CN after each clock edge.

The main advantage of the DE-TGPL compared to the DET latch-MUXs is its speed. An indication of the timing overhead of this pulsed latch can be obtained by observing that the D-to-Q path traverses only a single TG and an inverter. However, this timing overhead is somewhat degraded by the delay needed to generate the inverted clock pulse CN from CP, which causes an asymmetry between low-to-high and high-to-low setup and hold times.

The power consumption of the DE-TGPL is dominated by the clock activity, due to the large switching activity of the clock pulse generator. In addition, both pass gates in the XOR gate are simultaneously open for a short time whenever the clock is switching. As a result, a contention exists at each edge of the clock that causes an increase in overall power consumption. The clock load of the DE-TGPL consists of the input load of an unbuffered pass-transistor XOR gate. Therefore, it is considerably larger than the clock load of the corresponding SET TGPL, which consists of one static NAND gate and one inverter [6].

V. Advanced DETSE

In this section, two DET flip-flops are described that allow clock frequency reduction while maintaining comparable timing overhead and clock load to the conventional SETSE. In Section V-A, the DET conditional precharge flip-flop

(DE-CPFF) is presented, based on the generation of a transparency window after each clock edge, and reduction of the internal switching activity. In Section V-B, the SPGFF is introduced, which achieves low delay and low clock load by using two pulse generators, one for each edge of the clock, and a simple nonclocked second stage.

A. DET Conditional Precharge Flip-Flop

One approach for obtaining a DET flip-flop from a transparency window-based SET flip-flop is to generate a transparency window after each clock edge. The simplest way to do this is to generate an XOR logic function of the clock and the delayed clock. Another method, logically equivalent to the above, but simpler to implement, generates the signal CKD that switches low as a result of the rising edge of the delayed clock CK2, and switches high as a result of falling edge of the clock Clk. Logical AND of CKD and Clk gives the transparency window after the rising edge of the clock. Similarly, logical AND of CKD and the four-inverter-delayed clock CK4 provides the transparency window after the falling edge of the clock. Applying this method to the SET CPFF [18], we obtain the DE-CPFF [7], shown in Fig. 6(a). The internal node $\bar{S}$ evaluates (discharges) during these transparency windows if input $D = 1$. Outside of the transparency windows, the path from the node $\bar{S}$ to ground through the transistors M_1, M_2, M_3 is OFF, and either M_7 or the series M_8, M_9 are ON. Thus, the node $\bar{S}$ takes value of D NAND Q.

During the transparency windows, conditional evaluation of the node $\bar{S}$ takes place, based on the previous level of the output Q. If Q was low in the previous clock half-cycle, the node $\bar{S}$ was precharged high. In the transparency window, the node $\bar{S}$ switches low if D is high (either the path M_1-M_3-M_4 or the path M_2-M_3-M_4 is on). As a result, Q switches high via transistor M_{16}. If the input D is low, the node $\bar{S}$ remains high and Q remains low. If Q was high in the previous clock half-cycle, the node $\bar{S}$ took value of the inverted input D (M_4, M_5, and M_6). When a transparency window arrives, the high level of $\bar{S}$ causes Q to switch low (paths M_{11}-M_{13}-M_{14} and M_{12}-M_{13} -M_{14}). The low level of $\bar{S}$ has no effect to Q, as it was already high. Once the node $\bar{S}$ is low, it can return to the high level only if the input D is low. In other words, the node $\bar{S}$ does not exercise pre-charge-evaluate sequence in each clock cycle. Therefore, internal power consumed for the redundant pre-charge for the case $D = Q = 1$ is saved. Consequently, this flip-flop has the feature of conditional precharge and statistically reduces power consumption for low input activity.

Compared to nonconditional flip-flops [19], [20], the conditional precharge technique introduces the critical path for high-to-low transition at the input D ($1 \rightarrow 0$ transition of $D, 0 \rightarrow 1$ transition of $\bar{S}$, and $1 \rightarrow 0$ transition of Q in the transparency window). In order to capture the low data level, this $1 \rightarrow 0$ input data transition must occur early enough to ensure that the consecutive $0 \rightarrow 1$ transition of the node $\bar{S}$ arrives prior the closing of the transparency window in the second-stage latch. Therefore, the new critical path increases the setup time of the flip-flop, which in turn causes an increase of the timing overhead. Depending on the data switching activity, the detrimental effect of this delay increase may partially or completely cancel the energy improvement obtained from reducing internal switching activity.

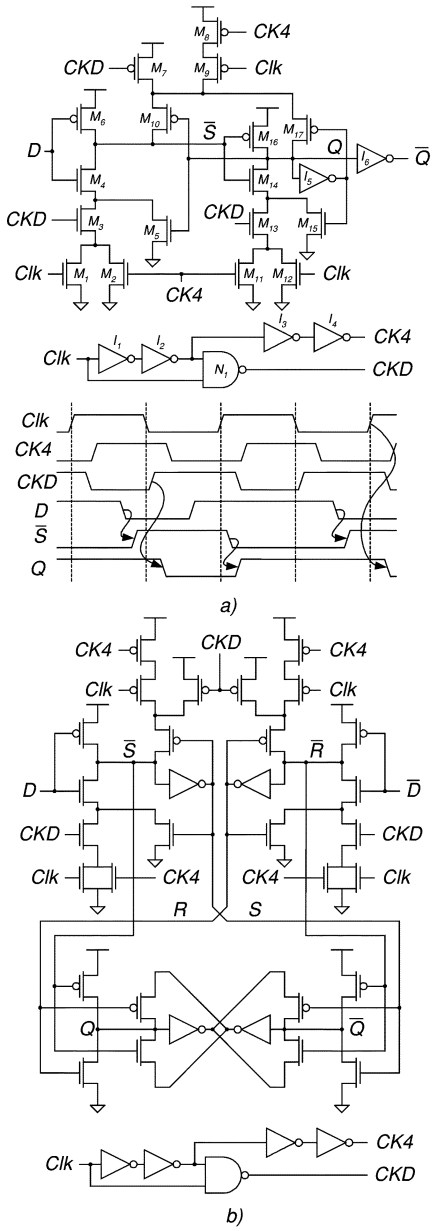

Fig. 6. DE-CPFF. (a) Single-ended (DE-CPFF). (b) Differential (DE-CPFF-D).

One way to avoid increasing the setup time is to use the differential CPFF. Fig. 6(b) shows the DE-CPFF-D that uses the local feedback (rather than the outputs $Q/\bar{Q}$) to maintain the logic levels of the nodes $\bar{R}$ and $\bar{S}$. This flip-flop uses differential pulse generator that creates pulses at the nodes $\bar{S}$ and $\bar{R}$, and the push-pull set-reset latch in the second stage [21]. Since the transparency window in the second-stage latch is eliminated, low-to-high and high-to-low setup times are equal and energy-delay tradeoff is improved compared to the single-ended DE-CPFF.

B. Symmetric Pulse Generator Flip-Flop

The SPGFF ([8]) consists of two identical pulse generators and the NAND gate in the second stage, shown in Fig. 7(a). Each

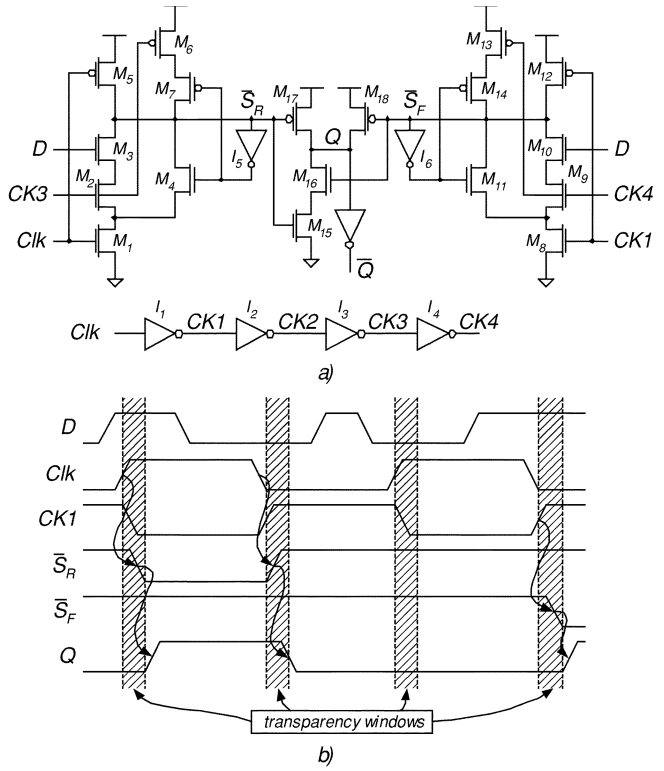

Fig. 7. SPGFF: (a) schematic and (b) timing diagrams.

of the two pulse generators captures data at one particular clock edge. The pulse-generating stages of the flip-flop work in the opposite phases of the clock: when the clock is high, the node $\bar{S}_F$ is precharged high, and the node $\bar{S}_R$ holds the value captured at the most recent rising clock edge; when the clock is low, the node $\bar{S}_R$ is precharged and $\bar{S}_F$ holds the value captured at the most recent falling clock edge. The output stage selects between $\bar{S}_R$ and $\bar{S}_F$. At any time, one of the nodes $\bar{S}_R$ and $\bar{S}_F$ holds the value of the input D captured at the most recent edge of the clock, while the other one is precharged high. Thus, the second stage does not need to latch the pulses $\bar{S}_R$ and $\bar{S}_F$, and it can be implemented using a simple static CMOS NAND gate.

For principle of operation of the SPGFF, refer to Fig. 7(b). The node $\bar{S}_R$ is precharged high during the time when the clock Clk is low. When Clk switches high, $\bar{S}_R$ is allowed to conditionally evaluate to low through the transistors M_1, M_2, M_3, depending on the level of input D (if $D = 0, \bar{S}_R$ stays high, otherwise it switches low). The node $\bar{S}_R$ is allowed to switch low only in the short transparency window following the rising edge of the clock in which $\mathrm{Clk} = \mathrm{CK3} = 1$. This transparency window is defined by the delay of the three inverters I_1-I_3 [Fig. 7(a)]. This feature makes setup time of the flip-flop negative and the short transparency window allows for clock uncertainty absorption. After the transparency window elapses, the logic level of $\bar{S}_R$ is preserved by the inverter I_5 and the transistors M_1, M_4, M_6, and M_7 during the time when the clock is high. The node $\bar{S}_R$ is precharged high after the falling edge of the clock Clk. Thus, the node $\bar{S}_R$ is allowed to switch from high to low only shortly after the rising edge of the clock and from low to high only after the falling edge of the clock. As a result, the transitions of the output Q or $\bar{Q}$ are synchronous with the clock edges.

The evaluation and the precharge phases of the node $\bar{S}_F$ are opposite to those of the node $\bar{S}_R$. The node $\bar{S}_F$ is precharged high when the clock Clk is high and the node CK1 is low. The node $\bar{S}_F$ evaluates at the falling edge of Clk, during the time when $\mathrm{CK1} = \mathrm{CK4} = 1$, defined by the propagation delay of I_2-I_4. Thus, the two first stages of the flip-flop alternately capture the data value D. At any moment, the sampled value of D at the most recent clock edge is held at either node $\bar{S}_R$ or $\bar{S}_F$, while the other of $\bar{S}_R$ and $\bar{S}_F$ is precharged high. Since the second stage of the SPGFF is a static NAND gate (transistors $M_{15}, M_{16}, M_{17}, M_{18}$), Q takes the value S_R when Clk is high ($\bar{S}_F = 1$), and S_F when Clk is low ($\bar{S}_R = 1$). Thus, at any moment, Q takes the value of D sampled at the most recent edge of the clock, which provides the functionality of DETSE.

The critical path of SPGFF consists of a single domino-like gate, whose first stage is dynamic and second stage is the static NAND gate M_{15}-M_{18} from Fig. 7(a). Thus, the static output is available after two fast logic stages. However, as the nodes $\bar{S}_R$ and $\bar{S}_F$ precharge and evaluate at each clock edge even when D and Q are constant high, the internal switching activity is high. In addition, if $D = Q = 1$, there exists a short overlap between $\bar{S}_R$ and $\bar{S}_F$ switching to opposite logic level after both edges of the clock. This overlap falsely drives the node Q low, causing a small glitch. Typically, the glitch after rising edge of the clock is negligible, whereas the glitch after the falling edge of the clock may be more pronounced due to the overlap between $\bar{S}_R 0 \rightarrow 1$ and $\bar{S}_F 1 \rightarrow 0$ transition. The largest simulated magnitude of this glitch over all process corners, temperature and zero load at the output, is smaller than 20% $\mathrm{V_{DD}}$. In order to ensure scalability over different processes, it is possible to eliminate this glitch using delayed precharge technique described in [22].

VI. Results

This section shows simulated results for DETSEs discussed in Sections IV and V. DETSEs are compared to the corresponding SETSEs in order to evaluate the performance potential of dual-edge clocking. The transmission-gate (TGLM) and the $\mathrm{C^2MOS}$ latch-MUX structures are compared to the transmission-gate (TGMS) and the $\mathrm{C^2MOS}$ master-slave latches. The DE-TGPL is compared to single-edge transmission-gate pulsed latch (SE-TGPL). The DE-CPFF and DE-ACPFF-D are compared to the single-edge conditional precharge flip-flops (SE-CPFF and SE-ACPFF-D).

As shown in Section II, DETSEs yield optimal performance if they operate with the optimal clock duty cycle. However, this assumption poses a difficult requirement to the system, and it may result in complex clock distribution network. Our goal is to estimate the performance of DETSEs assuming the same clock distribution as in SET systems. For this reason, the simulation was performed for fixed duty cycle of 50%, thus taking into account the performance degradation due to nonoptimal duty cycle. For the optimization and the performance evaluation of DETSEs, the timing metric is used that corresponds to the time taken from the clock half-cycle, assuming 50% clock duty cycle, given by (16). The timing penalty due to the duty cycle variation

TABLE I
SUMMARY OF THE STORAGE ELEMENTS CHARACTERISTICS

DETSE	TGLM	C^2MOS-LM	DE-TGPL	SPGFF	DE-CPFF	DE-CPFF (diff)
delay [ps]	171.37	210.33	124.65	133.37	128.52	95.03
setup time rising [ps]	35	50	-55	-35	-35	-35
setup time falling [ps]	40	45	-50	-45	-35	-35
hold time rising [ps]	15	65	130	75	80	75
hold time falling [ps]	65	90	110	105	115	115
race immunity [ps] [1]	21.27	42.04	-23.39	6.26	23.58	8.41
optimal duty cycle [%] [2]	49.97	49.79	50.33	49.77	49.08	48.99
delay @ optimal DC [ps]	170.35	206.81	122.18	132.38	125.95	92.06
number of transistors [3]	26	20	24 (12)	32 (8)	33 (12)	46 (12)
total transistor width [μm] [4]	27.46 (+50.38%)	24.6 (+0.82%)	20.36 (-6.61%)	27.64	30.32 (+29.35%)	35.64 (+34.8%)
leakage current [μA] [4,5]	3.99 (+6.2%)	5.05 (+19.5%)	5.12 (+20.1%)	5.45	5.95 (+25.2%)	7.05 (+27.3%)
input load [fF] [6]	6.26 (15.01)	7.43	4.62 (16.54)	4.26	5.78	2 x 5.02
clock load [fF] [6]	12.23	6.40	6.07 (15.05)	4.89	8.39	9.57
internal power [μW] [2,7]	14.02	14.47	22.38	21.72	19.37	21.79
total power [μm] [2,7]	21.53	18.47	29.47	24.53	24.02	27.45
EDP [10^{-24}Js] [2,7]	7.38	7.76	7.34	6.54	6.18	5.22

[1] race immunity is defined as minimum clock-to-output delay minus hold time
[2] f_{CLK}=250MHz
[3] in parentheses is number of transistors in clock generator (where applicable)
[4] in parenthesis is change compared to the corresponding SETSE (where applicable)
[5] fast process, VDD=1.32V, T=110°C
[6] in parentheses is the input load including load of the internal node that input drives through the transmission gate (where applicable)
[7] 25% data activity

is not taken into account. The optimal duty cycle at 250 MHz, and the timing overhead for this optimal duty cycle are shown in Table I.

The DETSEs that employ a pulse generator (flip-flops and pulsed latches) can be used with another power- and area-saving technique, which consists of sharing the pulse generator among N storage elements [25]. The pulse generator and the storage elements that use its output must be placed close to each other to avoid distortion of the clock pulse. This method reduces the power and the area of the circuit for a factor smaller than N, since the shared pulse generator must be larger than the original pulse generators, but still larger than 1 (for sufficiently large N), as the original per-CSE pulse generators are typically forced to waste area and power for driving lightly loaded nodes with minimum-size transistors, dictated by the design rules of the technology. The dual-edge clocking does not restrict the use of sharing the pulse generator, and the two can be used together for even further power savings. For a more detailed discussion on how sharing the pulse generator affects the energy-performance tradeoff, refer to [25].

The storage elements are simulated in 0.11 μm technology [23], with power supply voltage of 1.2 V, and temperature $\mathrm{T} = 25°\mathrm{C}$, unless specified otherwise. Clock frequency is 500 MHz for SETSEs and 250 MHz for DETSEs. The inverters driving the storage elements were sized so that their input capacitance is four times smaller than their load (FO4 load), thus fixing the clock and data signal rise and fall times, and loaded with 14 minimum size inverters, which is an equivalent of a moderate to high load that storage elements are typically required to drive in a VLSI design. Prior to simulation, the storage elements were optimized for energy-delay product (EDP), obtained as a product of the delay metrics discussed in Section II, average power consumption with 25% data activity, and clock period (half of the clock period for DETSE). The storage element is required to produce both polarities of the output, Q and $\bar{Q}$, and the slower output transition is chosen as the overall delay. The dissipation of the driving circuits for both clock and data inputs are taken into account when calculating power consumption. In this way, a measure of the load seen by driving logic imposed by the storage element is included in total energy, thus affecting overall performance. For more detailed description of the simulation testbench, refer to [11].

A. Comparison

Delay comparison between DETSEs and corresponding SETSEs is given in Fig. 8(a). From this figure, the delay of DET latch-MUXs and pulsed latches is somewhat larger, compared to their single-edge counterparts. The delay of DET flip-flops is comparable to corresponding SET flip-flops (– 9% to 21% difference). New developed DET flip-flops have similar delay to the DE-TGPL, and for about 1–1.5 FO4 lower delay compared to latch-MUXs. The DE-CPFF-D is the fastest simulated DETSE, with delay of about 2 FO4.

Fig. 8(b) presents the comparison of the average energy per cycle at 25% data activity. Fig. 8(b) shows that DETSEs are comparable to SETSEs in terms of energy consumption. Among DETSEs, latch-MUXs consume least energy, but their advantage over pulsed latches and flip-flops is considerably smaller in comparison to the advantage of master-slave latches over SET pulsed latches and flip-flops. This figure also shows that the internal power, which mainly depends on internal switching, is similar in DETSEs and corresponding SETSEs. Thus, the main energy savings of DETSEs comes from the clock energy, due to the operation at halved clock frequency. As shown in Fig. 8(c), DETSEs are generally comparable to SETSEs in terms of EDP. The energy-delay products of new developed DET flip-flops are 11%–33% smaller compared to the best conventional storage

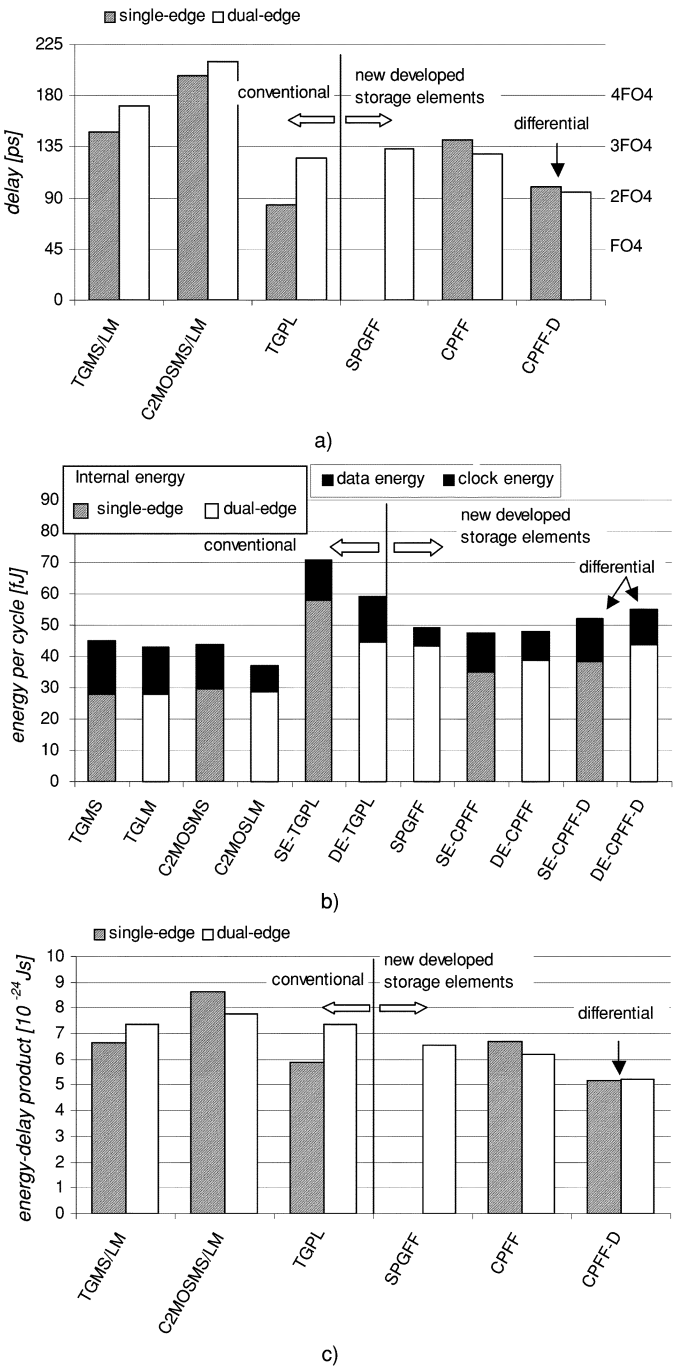

Fig. 8. Comparison between DET and SET storage elements. (a) Delay. (b) Energy per cycle. (c) EDP.

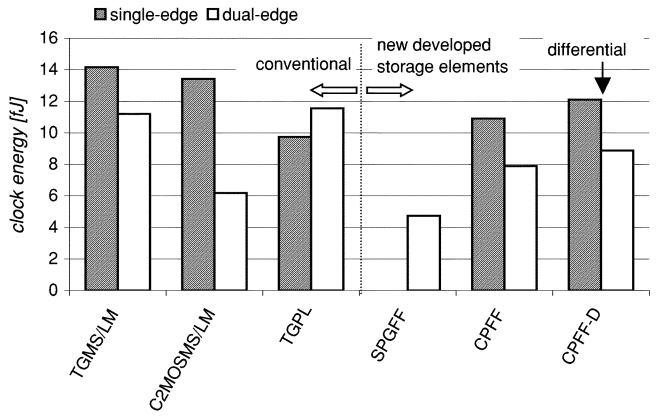

Fig. 9. Clock energy comparison between DET and SETSE.

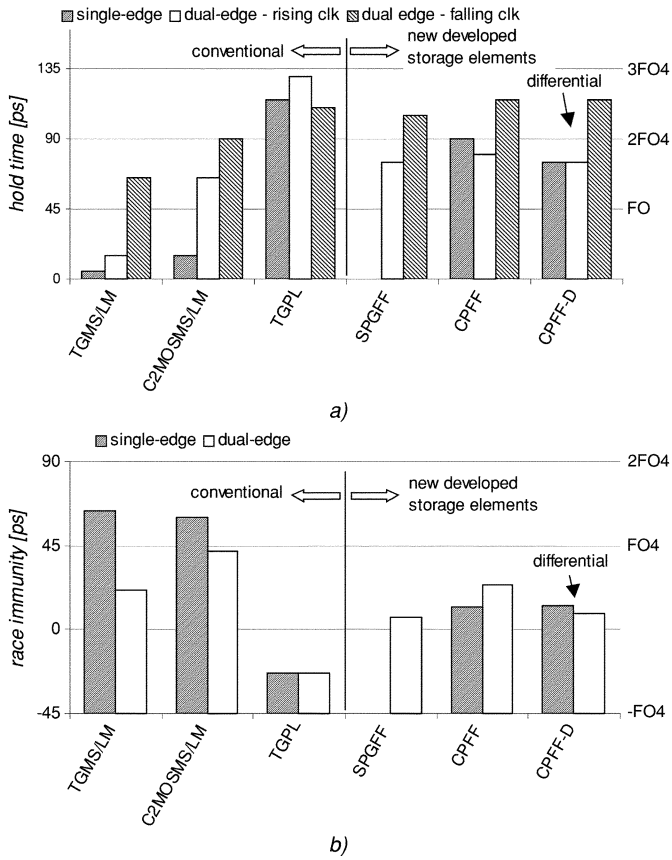

Fig. 10. Hold time and race immunity comparison between DET and SETSE. (a) Hold time. (b) Race immunity.

elements. Among the proposed flip-flops, the DE-ACPFF-D offers the best energy-delay tradeoff, due to symmetry between its low-to-high and high-to-low delays, fast second-stage latch, and low internal switching activity.

The clock energy comparison is shown in Fig. 9. This clock energy is the energy consumed by the clock driver to the storage element. As shown in Section III-A, it is a very important performance parameter of a DETSE, since it determines potential power saving in the clock distribution system by using dual-edge clocking. Clock energies of almost all simulated DETSEs are smaller compared to the corresponding SETSEs. The largest clock energy savings are obtained for the C^2MOSLM, due to clock transistor sharing (see Section IV-A), and the SPGFF, which uses clock only in the small first stage (see Section V-B). The clock energy of the SPGFF is 34%–77% lower compared to other simulated storage elements.

Fig. 10(a) shows the hold time and race immunity comparisons. Latch-MUX structures have the smallest hold time, and pulsed latch has the largest hold time. New developed DET flip-flops are in between these two groups. Typically, the hold time for one of the clock edges of a DETSE is comparable to the corresponding SETSE, whereas the hold time for the other clock edge is larger for about 1 FO4, which is the delay required to locally generate the second clock phase. As the clock-to-

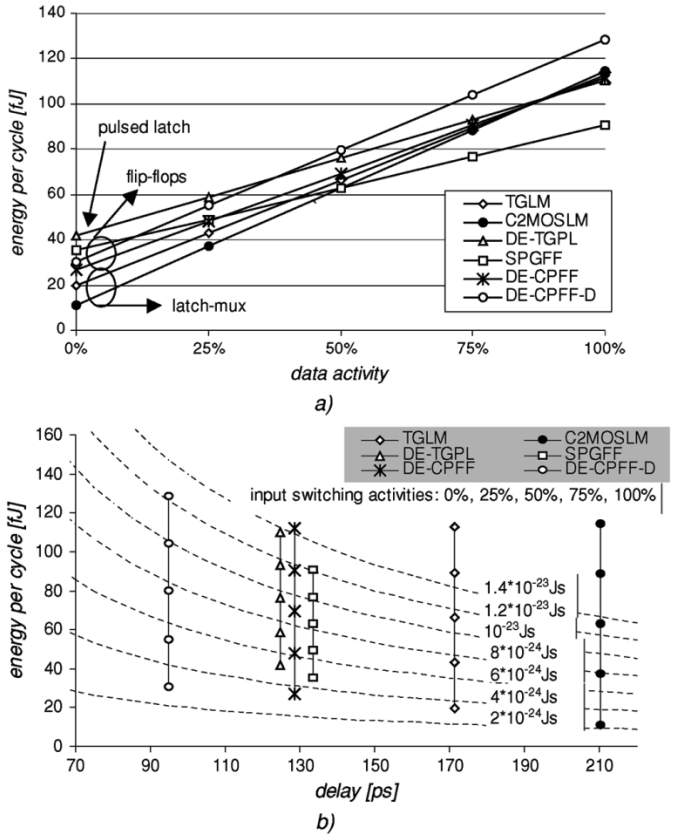

Fig. 11. Energy comparison of DETSE for different input switching activities: (a) Energy per cycle and (b) energy-delay tradeoff.

output delays of latch-MUXs are comparable to the master-slave latches, the latch-MUXs are less immune to fast paths compared to SET master-slave latches. The race immunity of latch-MUXs is comparable to new developed flip-flops, thus losing much of the advantage for use in the fast paths that master-slave latches have over SET flip-flops. The pulsed latch is least immune to races in single-edge and dual-edge clocking alike.

Fig. 11(a) shows the energy per cycle of DETSEs for different input switching activities, and Fig. 11(b) shows the tradeoff between this energy and delay. In these comparisons, storage elements are optimized for input switching activity of 25%. Latch-MUXs consume least energy for low input switching activity. In addition, as internal switching activities of latch-MUXs and conditional precharge flip-flops are largely data-dependent, their energy consumption is sensitive to the input switching activity. Thus, these storage elements are most suitable when the input switching activity is small, Fig. 11(b). In contrast, most heavily loaded internal nodes in the DE-TGPL and the SPGFF switch regardless of the input. Therefore, their energy consumption is much less sensitive to the input switching, which makes them preferable to latch-MUXs and conditional flip-flops only when the input switching activity is sufficiently high.

Table I shows the summary of the characteristics of evaluated DETSE and gives their comparison with respect to several other practical design issues. For all simulated DETSE, the deviation of the optimum clock duty cycle from the symmetrical clock is within $\pm 1\%$, and their timing overheads at 50% duty cycle are virtually the same as the minimum delays obtainable at the optimum clock duty cycle. The comparison of the size of the DETSEs, estimated using the number of transistors and total transistor width, shows that the new proposed DETSEs are likely to be similar size or slightly larger than the conventional DETSEs. Due to their increased circuit complexity, DETSEs tend to be larger than the corresponding SETSEs. In addition, the simulation under the worst conditions (fast process corner, 110°C, and with supply voltage 10% higher than the nominal V_{DD}), indicates that the leakage current of DETSE exceeds that of the corresponding SETSE by 6% to 27%. Note that this increase in the leakage current does not significantly affect total power of low-power systems, as the leakage of the storage elements is usually only a small portion of the total leakage [24]. Nevertheless, the overhead in area and leakage current of the DETSE must be weighed against the potential benefits available on account of halved clock frequency.

VII. Conclusion

For both low-power and high-performance systems, the power consumption became a primary design parameter. As clocking is responsible for roughly half of the power of the high-performance processors, use of a method that reduces this clocking power while not impairing the throughput is highly desirable. DET clocking may cut the clock load to half of that of the conventional SET strategies, and thus assist in future performance scaling, provided that the clock load and timing penalty of the DETSE are kept comparable to the original SETSE, and that the clock duty cycle is kept close to 50%.

For the first time, this paper presented the classification, consistent performance-based timing characterization, estimation of the savings in the clock distribution network, and system design issues with dual-edge clocking strategy. In addition, it presented a class of DET flip-flops with clock load, delay, and internal power consumption comparable to the fastest SETSE. The area overhead and leakage current increase are recognized as potential drawbacks of the DETSEs compared to the corresponding SETSEs. Simulation results indicate that DET flip-flops are suitable for the low-power and high-performance designs in the near future.

Appendix

In this appendix, the formula for total switching load in an ideal H-tree clock distribution tree, (22), is derived. The following are the assumptions:

- chip dimensions: s by s;
- total number of storage elements is M;
- ideal H-tree with FO4 drivers;
- number of levels in the H-tree is L, where Level L buffer is output of the clock generator (PLL), Level $L-1$ are the next four inverters, etc. The terminal buffers that drive local domains are designated Level 1;
- clock distribution in local domain driven by a Level 1 buffer is a straight wire from the common spine to the storage element, as shown in Fig. 4(a);
- uniform distribution probability for the location of storage element on chip;
- clock load of single storage element is C_{Clk}, and wire load per unit width is c_w. The wire resistance and electromigration effects are neglected, so that the widths of all wires are the same. If needed, this assumption can be

easily altered and similar derivation conducted to get the clock load formula using the same method as described below;
- formula calculates the total load driven by the Level L buffer [single inverter after the PLL in Fig. 4(a)].

The total load is divided into L parts, each driven by the buffers in the same level of clock distribution network. Further, we divide the load to the load that depends on the clock load of storage elements and the load that depends on wires. Consequently, in each local clock domain, load to Level 1 buffer consists of the storage element load and wire load (there is a total of $4^{\mathrm{L}-1}$ of Level 1 buffers):

- storage element load is the sum of all clock loads of individual storage elements. As there are $M/4^{L-1}$ storage elements in a local domain, the storage element load is $M * C_{\mathrm{CLK}}/4^{L-1}$.

In each local clock domain, wire load consists of the following:

- routing wires from the spine to the storage elements. With the assumption of uniform probability distribution of storage elements location on chip, the average length of the wires from storage elements to the spine depends only on the location of the spine and the size of the local domain (s^{L-1} by s^{L-1}). It is trivial to prove that the optimal location of the spine that minimizes the total length of these wires is in the middle of the domain, as shown in Fig. 4(a). In this case, the average length of routing wires from storage elements to the spine is $s/2^{L+1}$, and their total load is $c_w(s/2^{L+1}) \cdot (M/4^{L-1})$;
- load of the spine itself: $c_w(s/2^{L-1})$.

Load of single Level 2 buffer consists of the load imposed by Level 1 buffers and wiring in Level 2 (there is a total of 4^{L-2} of these buffers):

- assuming FO4 buffers, the input load of each Level 1 buffer is one fourth of its load. Since there are four Level 1 buffers per Level 2 domain, the total load imposed by these buffers equals one Level 1 load (sum of storage element and wire load);
- wire load of H-tree element in Level 2 is equal to c_w multiplied by the total length of the wire, equal to $3 * s/2^{L-1}$ [see Fig. 4(a)].

Load of Level 3 consists of the load imposed by Level 2 buffers and wiring in Level 3. There are 4^{L-3} Level 3 buffers. Similarly to the case of Level 2, the total buffer load is equal to the load driven by one Level 2 buffer, i.e., total buffer and wire load of Level 2 domain. Wire load of H-tree element in Level 2 is equal to c_w multiplied by the total length of the wire, which is equal to $3 * s/2^{L-2}$ [see Fig. 4(a)]. Load of Level L is the sum of the following:

- total load of Level $L-1$ (buffers);
- largest H-tree element wire load $(1.5s \cdot c_w)$.

In order to find the total clock distribution capacitance, including the load of the storage elements, the sum of all components from Level 1 to Level L should be found. An easy way to do this is to sum storage element-dependent load and the storage element-independent load separately. Total storage element-dependent load is

$$C_{\mathrm{Clk,tot}} = \frac{M}{4^{L-1}} \cdot C_{\mathrm{Clk}}(4^{L-1} + 4^{L-2} + \cdots 4^0) = \frac{\mathrm{MC_{Clk}}}{4^{L-1}} \cdot \frac{4^L - 1}{3}. \quad \text{(A.1)}$$

Storage element-independent load can be decomposed into two parts, $C_{\mathrm{WIRE},a}$ and $C_{\mathrm{WIRE},b}$, so that the total storage element-independent load C_{WIRE} equals $C_{\mathrm{WIRE},a} + C_{\mathrm{WIRE},b}$

$$C_{\mathrm{WIRE},a} = \frac{c_w s M}{2^{L+1} \cdot 4^{L-1}} \cdot (4^{L-1} + 4^{L-2} + \cdots 4^0) = \frac{c_w s M}{2^{L+1} \cdot 4^{L-1}} \cdot \frac{4^L - 1}{3}. \quad \text{(A.2)}$$

Component $C_{\mathrm{WIRE},b}$ itself can be decomposed into series of geometric progressions.

- Wire load of Level 1 (spines) and the input loads of all buffers in the H-tree due to the wire load of Level 1

$$C_{\mathrm{WIRE},b1} = \frac{c_w s}{2^{L-1}} \cdot (4^{L-1} + 4^{L-2} + \cdots 4^0) = \frac{c_w s}{2^{L-1}} \cdot \frac{4^L - 1}{3}. \quad \text{(A.3)}$$

- Wire load of Level 2 and the input loads of all buffers in the H-tree due to the wire load of Level 2

$$C_{\mathrm{WIRE},b2} = 3\frac{c_w s}{2^{L-1}} \cdot (4^{L-2} + 4^{L-3} + \cdots 4^0) = 3\frac{c_w s}{2^{L-1}} \cdot \frac{4^{L-1} - 1}{3}. \quad \text{(A.4)}$$

- Wire load of Level 3 and the input loads of all buffers in the H-tree due to the wire load of Level 3

$$C_{\mathrm{WIRE},b3} = 6\frac{c_w s}{2^{L-1}} \cdot (4^{L-3} + 4^{L-4} + \cdots 4^0) = 6\frac{c_w s}{2^{L-1}} \cdot \frac{4^{L-2} - 1}{3}. \quad \text{(A.5)}$$

- Wire load of Level L (no input load of the buffer included, since we are interested only in total load driven by the Level L buffer, not the load that Level L buffer imposes to the clock generator)

$$C_{\mathrm{WIRE},bL} = 3 \cdot 2^{L-2} \frac{c_w s}{2^{L-1}} \cdot \left(4^{L-(L-1)} + \cdots 4^0\right) = 3\frac{c_w s}{2}. \quad \text{(A.6)}$$

Summing $C_{\mathrm{WIRE},b} = C_{\mathrm{WIRE},b1} \ldots C_{\mathrm{WIRE},bL}$ yields

$$C_{\mathrm{WIRE},b} = c_w s \cdot \left[\frac{1}{3 \cdot 2^{L-2}} \cdot (5 \cdot 4^{L-1} + 1) - 3\right]. \quad \text{(A.7)}$$

Adding the (A.1), to (A.2) and (A.7), we obtain total switching capacitance of the H-tree, including the load of the storage elements

$$C_H = \frac{4^L - 1}{3 \cdot 4^{L-1}} M \cdot C_{\mathrm{Clk}} + c_w s \cdot \left[\frac{M}{3 \cdot 2^{L-1}} \cdot \left(\frac{4^L - 1}{4^L}\right) + \frac{5 \cdot 4^{L-1} + 1}{3 \cdot 2^{L-2}} - 3\right]. \quad \text{(A.8)}$$

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