A Low Power Symmetrically Pulsed Dual Edge-Triggered Flip-Flop*

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Abstract

A dual-edge triggered flip-flop suitable for low power applications is presented. HSPICE simulations conducted in 0.11u CMOS technology using 1.2V power supply voltage show that the proposed design is comparable in energy-delay product to high-performance single-edge triggered flip-flops while maintaining lower clock power. The Energy-Delay Product improvement of 14% and 50% smaller clock load compared to previously best published dual edge-triggered storage elements are demonstrated.

1. Introduction

Rapidly increasing clock frequency contributes directly to clock-related power consumption of microprocessors. The power consumed by the clock can reach half of the processor power, which is growing at roughly 20% per year. One approach to reduce clock-related power is use of dual-edge triggered storage elements (DETSE) in place of single edge-triggered storage elements (SETSE), similar to the use of DDRAM to increase memory bandwidth. Dual-edge clocking can achieve the same throughput at half the clock frequency and half the clock-related power consumption as compared to the use of single-edge clocked storage elements. However, in order to cash in on the power savings achieved in the clock distribution tree, these newly introduced storage elements should be comparable to their single-edged counterparts in power consumption and the load on the clock distribution tree.

Typically, a circuit required to capture data at both clock edges is more complex and/or slower compared to a SETSE. A challenge of DETSE design is to minimize this delay degradation in order to exploit the full potential of clocking at half the frequency. Also, in order to keep timing overhead low, dual-edge clocking requires tight control of the clock duty cycle and uncertainties of both clock edges. Thus, the ability to absorb clock uncertainties is essential.

In this paper, we present a new dual edge-triggered flip-flop that exhibits low latency and low power consumption. Section 2 describes the proposed flip-flop and its principle of operation. Section 3 reviews the simulation conditions and the testbench used to evaluate the performance and power consumption. Section 4 presents the results of the simulations and compares the proposed flip-flop with previously published single edge- and dual edge-triggered storage elements. Section 5 concludes the paper.

2. Symmetric Pulse Generator Flip-Flop

We present a new dual-edge triggered flip-flop (DETFF) that exhibits low delay and small power consumption compared to other storage elements. The new DETSE uses two symmetric pulse generator stages, each one responding to one particular transition of the clock, hence the name *Symmetric Pulse Generator Flip-Flop* (SPG-FF). The SPG-FF is shown in Fig. 1. Pulse generating stages X and Y of the flip-flop work in the opposite phases of the clock: when clock is high, node *Y* is pre-charged and node *X* holds the value captured at the rising edge; when clock is low, node *X* is pre-charged and *Y* holds the value captured at the falling edge. The output stage selects between *X* and *Y*.

The principle of operation of SPG-FF follows. As shown is Fig. 2, node *X* is precharged high during the time when the clock *CLK* is low. When *CLK* makes a low-to-high transition, *X* is allowed to conditionally evaluate to low through transistors Mn_1, Mn_2, Mn_3, depending on the level of input *D* (if *D*=0, *X* stays high, otherwise it switches low). Node *X* is allowed to switch to a low level only in the short time-window following the rising clock edge. This time window is defined by the delay of three inverters Inv_1-Inv_3 (Fig. 1). This feature makes the set-up time of the storage element negative and the short transparency window makes clock uncertainty absorption possible. After the transparency window elapses, the value of *X* is preserved while the clock is high, by inverter I_1 and transistors Mp_2, Mp_3, Mn_3 and Mn_4. Node *X* is again precharged high after the

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falling edge of the clock *CLK*. Thus, node *X* is allowed to switch from high to low only shortly after the rising edge of the clock and from low to high only after the falling edge of the clock. This ensures that the transitions of the output *Q* or $\overline{Q}$ are also synchronous with the clock edges.

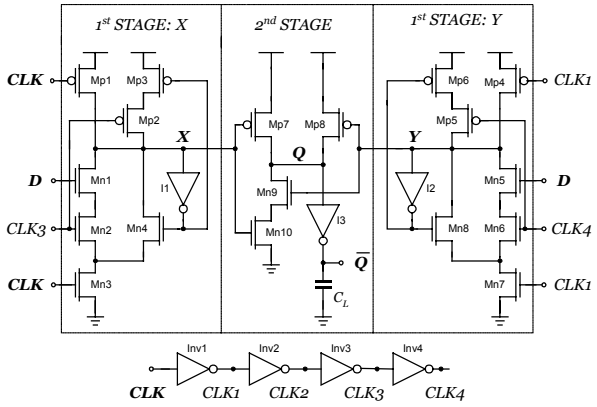

Fig. 1. Symmetric Pulse Generator Flip-Flop, SPG-FF

The evaluation and precharge phase of node *Y* are interchanged with respect to those of node *X*. Node *Y* is precharged high during the time *CLK* is high and node CLK_1 is low. It is then allowed to evaluate only after the falling edge of *CLK*, during the time window determined by the propagation delay of Inv_2-Inv_4. Thus, the two first stages of the flip-flop alternately capture the data value *D*. At any moment, the sampled value of D at the most recent clock edge is held at either node *X* or *Y*, while the other of *X* and *Y* is precharged high. Since the second stage of SPG-FF is a static NAND gate (transistors Mn_9, Mn_{10}, Mp_7, Mp_8), *Q* takes the value $\overline{X}$ when *CLK* is high (*Y*=1), and $\overline{Y}$ when *CLK* is low (*X*=1). Thus, at any moment, *Q* takes the value of *D* sampled in the most recent transparency window.

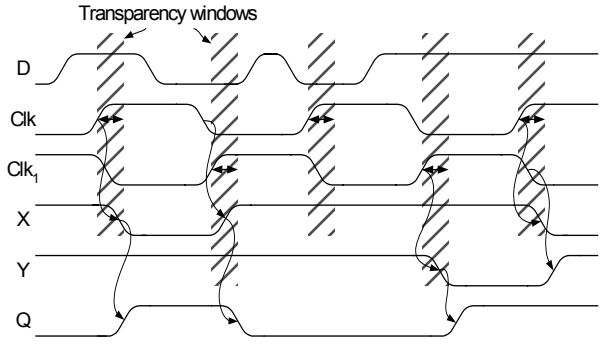

Fig. 2. Timing Diagrams of SPG-FF

An advantageous property of SPG-FF is that the critical path consists of a single domino-like gate whose first stage is dynamic (*1st STAGE: X* or *1st STAGE: Y*) and second stage is the static *NAND* gate from Fig. 1. Consequently, a static output is available after two fast logic stages. Normally, the transistors are sized so that each stage has about the same gain. In this case, speed is traded for power consumption.

3. Simulation Conditions

The proposed flip-flop was optimized (sized) for minimum energy-delay product (EDP) at 250MHz clock frequency, and then the delay and power consumption were compared with two previously presented DETSEs and three representative single-edge triggered storage elements (SETSEs). EDP is defined as the product of total power consumption, delay and maximum data rate at the clock frequency used. In order to attain a fair comparison, data throughput is maintained the same for DETSE and SETSE. This implies that the clock frequency of DETSEs is half of that of SETSEs. In this paper, all DETSEs were optimized for minimum EDP at 250MHz, and SETSE were optimized at 500MHz, which corresponds to the maximum data rate of 4ns for all storage elements.

The technology used was Fujitsu 0.11μm CMOS with VDD=1.2V and fan-out 4 delay (FO4) of 45ps. During optimization, and for comparisons, the output with worse EDP, *Q* or $\overline{Q}$, of each storage element was loaded with the equivalent of 14 inputs of minimal-size inverters with 2:1 P/N ratio. Note that this output is not necessarily the slower output, since the storage element that drives the slower output usually consists of more logic stages, thus having higher gain. This extra gain allows smaller transistor sizes, which results in power savings, possibly sufficient to outperform the same storage element loaded on the faster output.

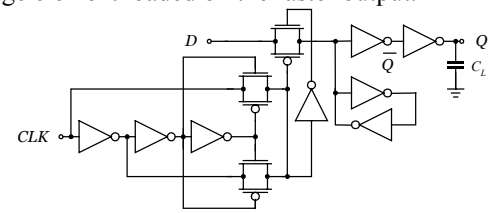

Fig. 3. Explicit-Pulsed Dual Edge Triggered Flip-Flop, ep-DSFF [3]

In the simulations, the sizes of the gates driving both data *D* and clock *Clk* inputs are chosen to have fan-out of 4 (FO4). In this way, the rise and fall times of signals at the nodes *D* and *Clk* are equal to those of FO4 inverter and thus similar to the rise/fall times in a realistic design.

The delay used for comparison was the larger of the timing overheads in two clock half-cycles of DETSE, as described in [1]: $t_D = \max(t_{D1}, t_{D2})$ where $t_{D1} = t_{su,f} + t_{CQr}$ and $t_{D2} = t_{su,r} + t_{CQf}$. Since tight duty cycle control is crucial for DETSE operation, it is assumed that a circuitry for the control of the clock duty cycle is implemented. Recent paper [2] presents a method for controlling clock duty cycle at 50%±0.5% at 433MHz. In order to maintain the fairness of the comparison with SETSE, a 10ps margin is added to both t_{D1} and t_{D2}, which is equivalent to increasing t_D by 10ps.

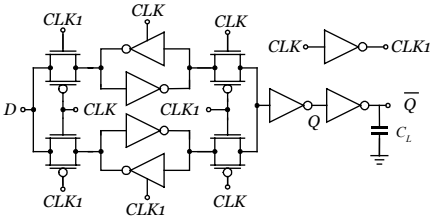

Fig. 4. Transmission-Gate Latch-MUX, TGLM [4]

Power consumption of a storage element is the sum of the internal power consumption (including the power needed to switch the loaded output) and the power dissipated by the drivers of clock and data inputs to the storage element. In this way, a measure of the load that the storage element presents to the clock distribution system and the preceding logic is taken into account. The power is measured at 25% data activity. Activity is defined as the percentage of data switching per clock capturing edge.

4. Comparisons and results

Other DETSEs used for comparison are the *explicit-pulsed dual-edge triggered static flip-flop* (ep-DSFF, Fig. 3) [3] and the *transmission-gate latch-mux* (TGLM, Fig. 4) [4]. Table 1 shows the comparison in terms of speed, clock power, total power and energy-delay product. The SPG-FF is 13% faster than the ep-DSFF (Fig. 5), and it consumes 23% less power. SPG-FF's overall EDP at 25% input activity is lower by 14% than TGLM and 35% than ep-DSFF as shown in Fig. 6.

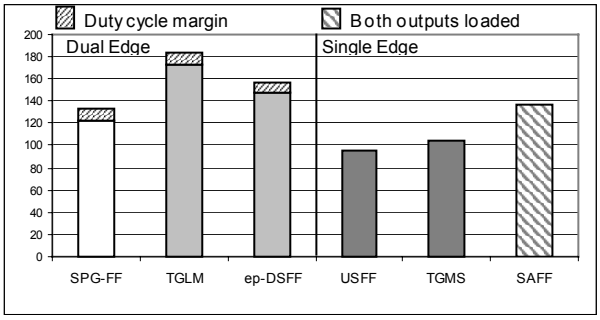

Fig. 5. Delay Comparison (delay in ps)

In order to illustrate the feasibility of the proposed flip-flop, we compare it with a group of representative SETSEs in terms of delay, power consumption and EDP. SETSEs used for comparison are: fast flip-flop used in Sun's UltraSPARC-III (USFF, [5]), a low power Transmission-Gate Master-Slave Latch (TGMS) used in the PowerPC processor [6] and a differential Sense-Amplifier Flip-Flop used in an Alpha processor (SAFF, [7,8]). In comparison with single edge-triggered storage elements, the SPG-FF is 28% slower (38% when the margin of 10ps for the clock duty cycle imperfections is taken into account). The power consumption improvement of 14-25% makes the EDP of the SPG-FF comparable to the best single-edge designs. Power can be traded for speed if needed by re-optimizing the design.

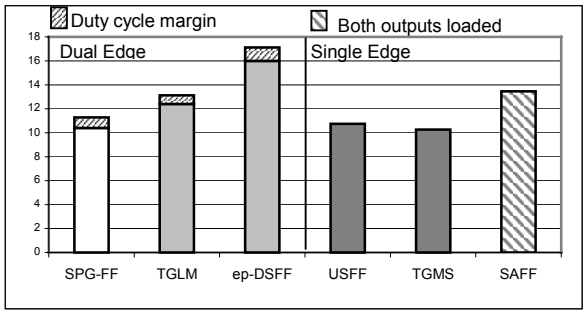

Fig. 6. EDP Comparison (EDP in Js×10-24)

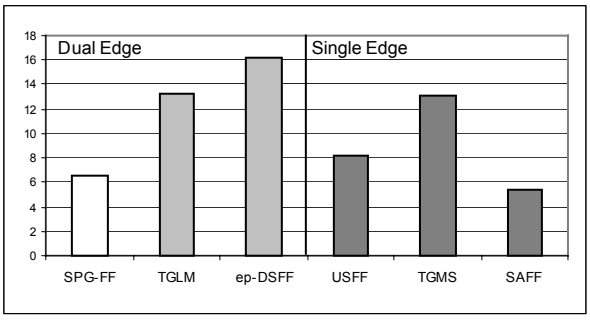

Fig. 7. Comparison of storage elements clock load (C_{CLK}, load in fF)

Note that the delay and EDP comparisons are performed at the level of single storage element. The major benefit of a DETSE is clocking at half the clock frequency of a SETSE, which may bring considerable power savings in the clock distribution network. Thus, the crucial parameter in determining potential advantage of DETSE is the total switching load (due to the storage elements, clock buffers and wires) for the single edge- and dual edge-triggered system. We find this load by estimating the load of a H-tree clock distribution network with L levels in a microprocessor die of size s x s with M storage elements. In this way, each Level L driver supplies the clock to an area of $s/4^{L-1}$ (local domain) that contains $M/4^{L-1}$ storage elements. In the local domain, the clock is distributed as shown in Fig. 8. c_W and C_{CLK} are wire capacitance per unit length and clock capacitance of a storage element, respectively. We neglect the wire resistance, so that the width, and thus capacitance, of the wires do not depend on the storage element clock load.

Under the above assumptions, it can be shown that the total load in the H-tree, including the clock load of storage elements is:

$$C_H = \frac{4^L - 1}{3*4^{L-1}} MC_{CLK} + c_W s\left[\frac{M}{3*2^{L-1}}\left(\frac{4^L-1}{4^{L-1}}\right) + \frac{1}{3} * \frac{5*4^{L-1}+1}{2^{L-2}} - 3\right]$$

First item in the right hand side of the above equation, call it C_{CLKtot}, is the portion of the H-tree capacitance that depends on the clock load of a storage element, and it can be approximated to $4MC_{CLK}/3$ if $4^L >> 1$. The second item of the same expression, C_{WIRE}, is the part of the clock distribution load that is independent of the clock load (the wire load and the buffers needed to drive it). If $M >> 4^L >> 1$, $C_{WIRE} \approx c_W sM/(3*2^{L-1})$.

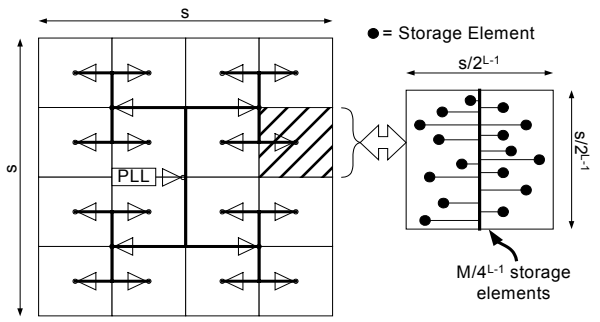

Fig. 8. H-tree clock distribution network

To estimate the power savings of dual edge clocking, we form the coefficient α, which is the ratio of the clock distribution switching power consumptions of DETSE- and SETSE- based systems:

$$\alpha = \frac{P_{DE}}{P_{SE}} = \frac{1}{2}\frac{(C_{WIRE} + C_{CLKtot,DE})}{(C_{WIRE} + C_{CLKtot,SE})} = \frac{1}{2}\frac{(1 + C_{CLK,DE}/W)}{(1 + C_{CLK,SE}/W)}$$

Here, $W = c_W s/2^{L+1}$ is the average capacitance of the wire needed to route the clock signal from the level L buffer to a storage element, and indices DE and SE correspond to dual edge and single edge clocking, respectively. In a typical design in today's technologies, C_{WIRE} (W) is usually much greater than C_{CLKtot} (C_{CLK}), in which case the saving is nearly 50%. For example, for a 5 level H-tree in 12x12mm die fabricated in the technology used in the simulations, the clock distribution power saving obtained by replacing evaluated SETSEs by SPG-FF is between 48.8% for SAFF and 55.4% for TGLM.

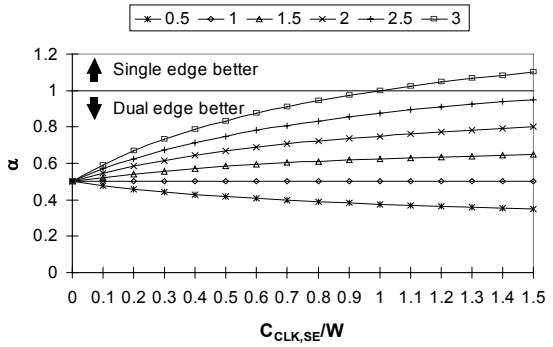

Fig. 9. Dual-edge vs. single edge H-tree power consumption The parameter is $C_{CLK,DE}/C_{CLK,SE}$

Fig. 9 presents clock distribution tree power consumption ratio α versus $C_{CLK,SE}/W$ for the above example of H-tree. From Fig. 7 and Table 1 it is seen that the clock load of SPG-FF is 50% or more lower than the clock loads of TGML and ep-DSFF and comparable to that of simulated SETSE. Thus, the expected power saving in clock distribution network is around 50% for any clock load to wire capacitance ratio. It should be noted that most high-performance designs, wire load is even more pronounced than in H-tree (e.g. clock grid) so that the saving that can be achieved by using proposed DETSE is even higher.

5. Conclusion

A new dual-edge triggered flip-flop, SGP-FF, is presented. The simulation results in 0.11um technology show an EDP and delay improvement over two previously published DETSEs of 14%, being comparable to the best single-edge designs, even when a timing margin for imperfections in clock duty cycle is taken into account. The clock load of the proposed flip-flop is similar to the clock load of SETSEs used in the high-performance processor designs, allowing power savings of about 50%. This makes this DETSE a viable option to be used in both high-performance and low-power systems.

6. References

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Table 1. Simulation Results at a=25% data activity, $t_{su,r}$ and $t_{su,f}$ are the setup times for rising and falling *CLK*, t_D = max (t_{D1}, t_{D2}) where t_{D1} and t_{D2} are data delays for half-cycles where CLK=0 and CLK=1. Duty Cycle margins added in parentheses

Storage Element	$t_{su,r}$ [ps]	$t_{su,f}$ [ps]	t_D [ps]	Internal Power [μW]	Clock load [fF]	Total Power [μW]	*EDP* [$\times 10^{-24}$ Js]
SPG-FF	-19	-39	123 (137)	18.41	6.61	21.18	10.4 (11.27)
TGLM	46	43	173 (183)	11.45	13.19	17.94	12.4 (13.13)
ep-DSFF	-17	-20	147 (157)	20.25	16.25	27.24	16 (17.11)