International Conference on Computer Design, ICCD 2001, Austin, Texas, September 23-26, 2001

Timing Characterization of Dual-Edge Triggered Flip-Flops

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Abstract

A novel timing characterization for dual-edge triggered flip-flops is presented in this paper. This characterization takes into account the real overhead taken from the clock cycle by the flip-flops. Our study shows the correctness of this new metrics when compared against data-to-output delay.

1. Introduction

Recent technological, circuit and architectural development lead to outstanding performance and frequency increase of VLSI processors [1, 2]. However, clock frequency in excess of 1GHz is related to a number of drawbacks. Most significant problem is power consumption. Clock-related power consumption alone could reach in excess of 30-40% of the total power of today's microprocessors as reported in [1, 2].

Another problem is related to the control of clock uncertainties: *clock jitter* and *clock skew*. Most designs attempt to cope with these phenomena by using high-quality clock generators and balanced clock distribution networks. With growing clock frequency, both clock jitter and skew occupy increasingly significant part of the clock cycle. Degeneration of clock waveforms due to electromagnetic coupling and cross-talk with the logic paths on the chip represent other problems.

Alternative state element design capable of capturing data on both clock events (rising and falling edge) has been receiving increased attention [3, 4]. These designs are referred to as Dual-Edge Triggered Flip-Flops (DETFF). Main advantage of DETFF is the possibility of obtaining the same data throughput with one half of the clock frequency, thus relaxing the power and clock uncertainty requirements. Simple analysis shows that halved clock frequency would reduce clock-related power to about the half of the original design, and significantly reduce total power consumption in the VLSI design. Less aggressive clock subsystems can be built, further reducing power consumption and allowing for the design towards minimizing the clock uncertainties.

DETFF use brings two problems: one is increased complexity of the design and the second is in the lack of precise control of the clock duty cycle.

Given a strong potential use of the clocking strategy incorporating DETFF, the timing characterization of DETFF's is needed. Current DETFF designs are characterized by their maximum data rates [5, 6, 7] or data-to-output delays [3], which we find not to be proper.

This paper proposes simple timing characterization of dual-edge flip-flops. This characterization further develops set-up time requirements described in [8]. The example of proposed delay characterization and the comparison with conventional (data-to-output) metrics for the dual-edge flip-flop design [7] is given.

2. Timing Characterization of DETFF's

The proposed characterization is related to flip-flops used in high-performance data-path applications. In a typical pipeline stage the logic processes data supplied by triggering flip-flops and delivers the results to the capturing flip-flops. This logic path environment dictates the system performance. Simple intuition is that the faster the flip-flip, the more time is left for the logic operations. The time taken away from the cycle by the flip-flop is the sum of the clock-to-output time at the beginning of the cycle and the set-up time at the end of the cycle, defining the data-to-output timing parameter [8].

Clock-to-output characteristic of a flip-flop typically has the shape presented in Figure 1. Two parts of characteristic can be distinguished: *safe*, where clock-to-output characteristic is constant, and *failing*, where the data arrives too close to the clock edge so that the flip-flop clock-to-output delay increases, until the flip-flop fails to capture the data.

If dual-edge triggered flip-flops are used, two clock-to-output curves are obtained – one corresponding to the rising edge of the clock and the other one corresponding to the falling edge of the clock. These two characteristics are independent from each other and generally are not the same.

Dual-edge triggered flip-flop behaves differently in two halves of clock period as shown in Fig. 2. If the data is captured on rising edge of FF1 and the clock uncertainties are neglected, the following relation can be written:

$$t_{CQ1,LH} + t_{LOGIC} + t_{D-CLK2,HL} \le T_{CLK} / 2$$

If the data is captured on the falling edge of FF1, the following relation stands:

$$t_{CQ1,HL} + t_{LOGIC} + t_{D-CLK2,LH} \le T_{CLK} / 2$$

Here, t_{CQ1} represents the clock-to-output time, $t_{D\text{-}CLK}$ is the time between the arrival of D and the arrival of clock, t_{LOGIC} is the time needed for the logic between the flip-flops to evaluate, and LH and HL indices stand for low-to-high and high-to-low cases, respectively.

The goal is to maximize the time left for the logic function (t_{LOGIC}), while satisfying timing requirements of the flip-flops. Thus, the data arrival for the flip-flop can be delayed as long as its clock-to-output time does not increase significantly (Fig.2.). Otherwise, the timing budget of the next logic stage is negatively affected.

This leads to definition of two functions of data-to-clock times ($t_{D\text{-}CLK,LH}$ and $t_{D\text{-}CLK,LH}$) that describes the time taken from two half-cycles of the clock (flip-flop overheads), analogously to single-edge triggered flip-flop:

$$t_{D1} = t_{CQ,LH} + t_{D-CLK,HL}$$

$$t_{D2} = t_{CQ,HL} + t_{D-CLK,LH}$$

The relevant flip-flop timing parameter for dual-edge triggered flip-flop, describing its maximum overhead is:

$$t_{FF} = \max(t_{D1}, t_{D2})$$

t_{FF} a function of two independent variables, $t_{D\text{-}CLK,LH}$ and $t_{D\text{-}CLK,HL}$, since clock-to-output delays are direct functions of the two.

Timing characterization of the dual-edge triggered flip-flop, therefore, is the process of finding two independent parameters, $t_{D\text{-}CLK,LH}^{opt}$ and $t_{D\text{-}CLK,HL}^{opt}$, for which the function t_{FF} takes the minimal value. Minimum t_{FF} is the minimal overhead of the flip-flop. $t_{D\text{-}CLK,LH}^{opt}$ and $t_{D\text{-}CLK,HL}^{opt}$ are the timing parameters of the dual-edge triggered flip-flop, referred to as optimal set-up times. It should be noted that if this timing metrics is used in conjunction with power consumption in order to obtain PD^XP metrics, the optimal set-up times may experience a shift towards *safe* region of clock-to-output characteristics

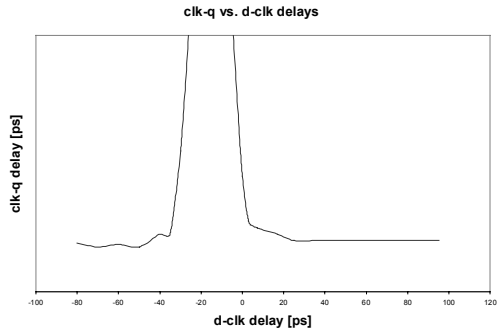

Fig. 1. Typical clock-to-output characteristic

(to the left) due to less power consumption in that part of the curve.

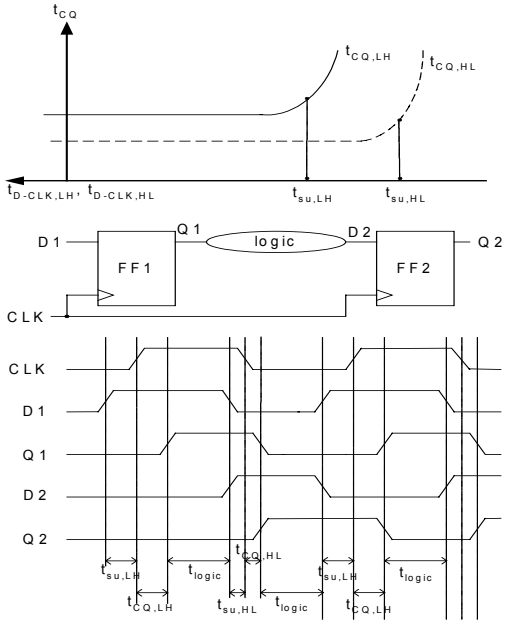

Fig. 2. Dual-edge triggered flip-flop timing diagrams

It can be concluded that in dual-edge case, simple flip-flop propagation time from input to output (data-to-output time) is not the correct measure of the flip-flop overhead taken from the half-cycle. The only case where the data-to-output time is equal to flip-flop overhead is when two clock-to-output characteristics coincide, and the symmetry between clock-to-output characteristics exists.

Figure 3 illustrates the process of obtaining the pair of optimal set-up times. Clock-to-output characteristics are given in Figure 3a. Figure 3b shows the plot of t_{D1} and t_{D2} (as defined above) as functions of data-to-clock time for the falling clock edge ($t_{D\text{-}CLK,HL}$), with data-to-clock time for the rising clock edge ($t_{D\text{-}CLK,LH}$), as a parameter. Function t_{D1} is the sum of $t_{D\text{-}CLK,HL}$ and $t_{CQ,LH}$. The time $t_{CQ,LH}$ is a function of $t_{D\text{-}CLK,LH}$ which is a constant for a single plot of t_{D1}. Therefore, t_{D1} is linear function of $t_{D\text{-}CLK,HL}$, with the slope of 45° (Figure 3b). Function t_{D2} is the sum of the clock-to-output characteristic for falling edge and the constant ($t_{D\text{-}CLK,LH}$). When the parameter $t_{D\text{-}CLK,LH}$ changes for $\Delta t_{D\text{-}CLK,LH}$, t_{D1} characteristic shifts vertically for the same amount, while t_{D2} shifts for

$$-\Delta t_{CQ,LH} = -(t_{CQ,LH}(t_{D\text{-}CLK,LH,new}) - t_{CQ,LH}(t_{D\text{-}CLK,LH,old}))$$

Function $t_{FF}=\max(t_{D1}, t_{D2})$ reaches its minimum, t_{min}, for $t_{D\text{-}CLK,LH}=t_1$, $t_{D\text{-}CLK,HL}=t_2$. Therefore, $t_{D\text{-}CLK,LH}^{opt}=t_1$, $t_{D\text{-}CLK,HL}^{opt}=t_2$, and timing overhead of the flip-flop is t_{min}.

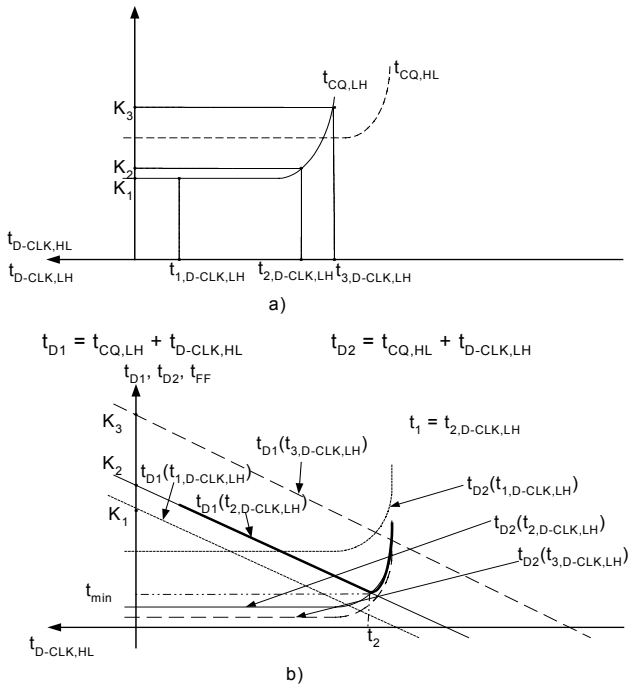

Figure 3. Process of obtaining minimum DETFF timing overhead

The example of a scenario where the data arrival times are set to optimal set-up times with respect to the clock edges and corresponding flip-flop delays, is shown in Figure 2. It can be seen that the same amount of time in two half-cycles is left for logic evaluation, which is where minimum overhead should reside.

Thus, the timing parameter optimization for the DETFF should be done in the way that minimizes cross-sums ($t_{D\text{-}CLK,LH}+t_{CLK\text{-}Q,HL}$ and $t_{D\text{-}CLK,HL}+t_{CLK\text{-}Q,LH}$). Specifically, if the set-up time for the falling-edge is larger than the set-up time for the rising-edge, it is more important to minimize the clock-to-output time for the falling-edge. Similarly, if the set-up time for the raising-edge is larger than the set-up time for the falling-edge, we should minimize the clock-to-output time for the raising-edge. Therefore, it is not needed to operate with identical clock-to-output characteristics.

It is important to have the clock waveform with duty cycle as close as possible to 50% since any deviation from it will directly add to either t_{D1} or t_{D2}, change optimal set-up times and increase the minimum of t_{FF}.

3. Simulations

The simulations are performed with power supply voltage of 1.8V and temperature T=27°C. Technology used is 0.18μm by Fujitsu. Clock frequency used in all simulations is 250MHz.

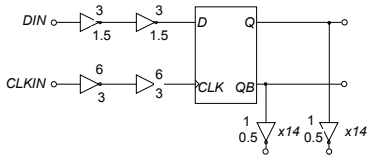

Figure 4. Simulation Testbench

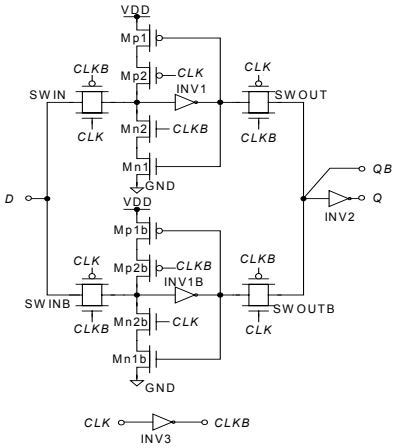

Figure 5. Dual-edge triggered flip-flop used for the metrics comparison

The test bench used for simulation is given in Figure 4. Parameter used as a figure of merit of the flip-flops is Energy-Delay Product (EDP). It is obtained as a product of device delay (t_{FF} or t_{DQ}) and average flip-flop power at a reference frequency with 50% data activity with respect to maximum throughput. Dissipation of driving circuits for both clock and data is taken into account when calculating power consumption. In this way, the load

imposed by the flip-fop to the driving logic and clock drivers is calculated in the total performance.

4. Results

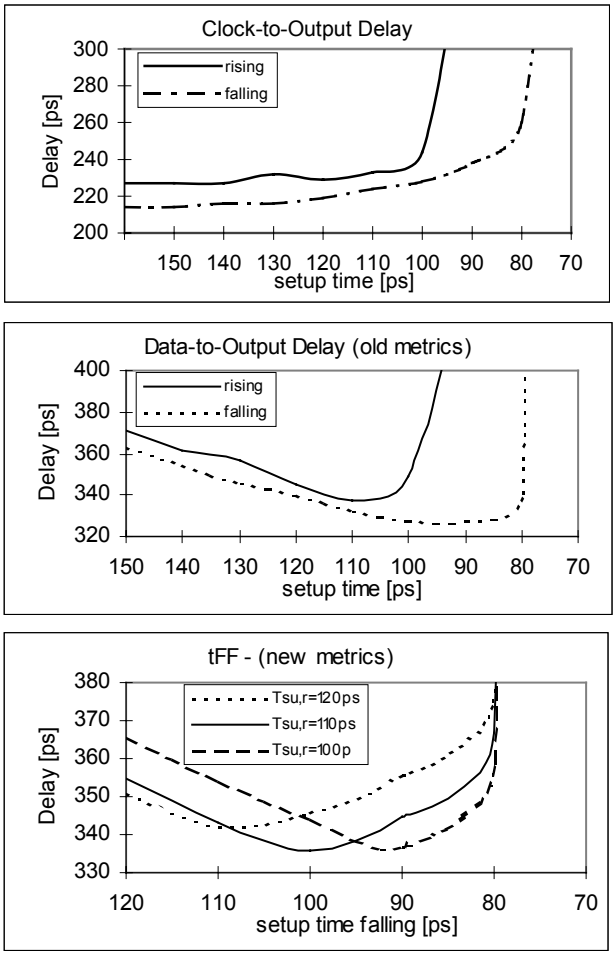

Figure 6. Simulation Results

The dual-edge triggered flip-flop used for the evaluation of proposed metrics is shown in Figure 5 ([7]). This flip-flop is the dual-edge version of Transmission-gate flip-flop (referred to as PowerPC flip-flop in [8]). The simulated clock-to-output characteristic is shown in Figure 6. It can be seen that the curves for rising and falling edge case do not coincide (high-to-low case has smaller stable t_{CLK-Q} and fails for smaller t_{D-CLK}).

Table 1. Simulation results

metrics	$t_{su,r}$ [ps]	$t_{su,f}$ [ps]	Delay [ps]	EDP [fJ/250MHz]
old	110	110	337	44.5
new	110	100	335	44.3

The timing metric adopted from the single-edge case (data-to-output delay) and the family of t_{FF} curves is given in Figure 6. The insight in the peak performances of the flip-flop with respect to the two metrics can be obtained from the Table 1. It can be seen that proposed metrics uses the set-up time for falling clock edge that cannot be exercised if the traditional metrics is used.

Even though it is not possible to get worse timing overhead using proposed metrics compared to data-to-output delay, this is not the fundamental point and it is not the reason why the proposed metrics should be used. Instead, it is the correctness in which it reflects the time flip-flop takes away from the half-cycle. Even when min(t_{FF}) metrics does coincide with data-to-output delay, it gives the insight in the nature of the timing overhead and understanding the directions for flip-flop optimization, so it should be used instead.

5. Conclusion

The novel timing metrics for characterizing the dual-edge triggered flip-flops is proposed. It is based on the real flip-flop overhead over the half-cycle. Basic timing parameters of the dual-edge flip-flop analogous to the single-ended case are defined. The simulated results illustrate the correctness of the proposed characterization.

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