

20.2 A Low Power SOI Adder Using Reduced-Swing Charge Recycling Circuits

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Power reduction is a critical requirement in modern VLSI design due to increasing operating frequencies and circuit densities, and the emergence of portable applications. Decreasing the supply voltage, V_{DD} , is the easiest way to reduce power consumption in CMOS circuits because switching power is proportional to V_{DD}^2 for rail-to-rail logic swing. However, reducing V_{DD} degrades circuit speed due to the super-linear reduction of transistor current. Lowering transistor threshold voltage, V_{th} , helps to recover this speed degradation; however sub-threshold leakage current increases exponentially with decreasing V_{th} , resulting in battery-draining quiescent power consumption with V_{th} less than about 300mV. Circuit techniques are needed to achieve lower power consumption without speed degradation. The low-power CMOS SOI circuit configuration reported here, low-swing charge recycling (LSCR), uses differential pass-transistor logic, a low voltage swing, and charge recycling to save power.

The dynamic power consumption in CMOS is proportional to both the logic swing, V_{sw} , and to V_{DD} . Reducing V_{sw} reduces power consumption without lowering V_{DD} , thereby maintaining the transistor drive current and avoiding speed degradation. Low swing circuit techniques are widely used in memory designs. For example, complementary bit line inputs with swing lower than 100mV are differentially detected by a sense amplifier, which speeds up memory access. The low swing technique is also applied in dual-rail data path logic [1].

Another technique for lowering power consumption is charge recycling [2]. In a typical CMOS circuit, all charge stored at the output node is dumped to ground when the output state changes. A charge recycling circuit can re-use the charge from the previous cycle to reduce the power associated with the nodes involved in charge recycling by half.

Figure 20.2.1a shows an XOR gate implemented in the LSCR structure. Figure 20.2.1b shows the same gate implemented in the previous nMOS dynamic differential logic [1]. Referring to Figure 20.2.1a and the timing diagram in Figure 20.2.2a, the LSCR structure evaluates when $CLK=1$, pulling the OUT signal to $V_{DD}-V_{th}$ and \bar{OUT} to 0, or vice-versa, depending on the inputs. The OUT and \bar{OUT} signals can be connected to succeeding stages of pass-gates. Note that evaluation is static – all nodes are actively driven. The final stage is latched in a differential sense amplifier flip-flop [2] (not shown.) When $CLK=0$, the tri-state gates driving into the nMOS pass gates are shut off, and the equalization FET is activated, resulting in charge sharing between OUT and \bar{OUT} , precharging both nodes to approximately $(V_{DD}-V_{th})/2$. Referring to Figure 20.2.1b and Figure 20.2.2b, the previously published dynamic structure [1] also evaluates when $CLK=1$, but charges one output to $V_{DD}-V_{th}$, while the complementary output is left floating at ground. When $CLK=0$, both outputs are discharged to ground. In practical datapath circuits, the pass gate chain can be long, and many wires must be wired through the datapath, making protection of the dynamic node from capacitive coupling difficult. Capacitive coupling into the dynamic node can degrade speed and/or cause operational failure.

Both the LSCR structure and the previous dynamic structure can be fabricated in bulk CMOS or SOI. However, SOI has a benefit to both circuits. In the bulk implementation, the body voltage of the nMOS devices in the pass chain is fixed at ground, causing V_{th} to increase by the body effect as the source and drain voltages are raised during evaluation. In contrast, when both the source and drain voltages are raised in an SOI nMOS pass chain, the capacitively-coupled floating body follows, resulting in less body effect and less V_{th} increase compared to bulk devices. Lower nMOS V_{th} in the pass chain speeds up both circuits.

LSCR is applied to a carry skip adder. Figure 20.2.3 shows a 4b carry skip adder with conflict-free carry bypass [3]. Each generate signal ($G_i, \bar{G}_i, i=0..3$) drives into the carry chain through low-swing tristate inverters, and propagate signals ($P_i, \bar{P}_i, i=0..3$) drive the gates in the nMOS pass-transistor network. Carry signals propagate through this network and the differential voltage between Cout and \bar{Cout} is amplified and latched in a sense amplifier flip-flop [3]. Note that there is no contention between the bypass transistor gated by $P_0P_1P_2P_3$ and the local carry chain. The sum signals are generated by pass-gate XORs and are also latched in sense amplifier flip-flops. A wider adder is designed by serially connecting this 4b adder module. An experimental 64b adder is formed by serially connecting 16 4b adder modules, and fabricated it in 0.08 μ m SOI CMOS technology. An identical SOI adder is formed with all FET bodies contacted. A micrograph of the test circuit is shown in Figure 20.2.4. The adder with floating body devices is 23x840 μ m².

The simulation results in Figure 20.2.5 show the benefit of the floating body in 0.08 μ m SOI. In the figure, add delay is plotted vs. V_{DD} for a 64b adder both with contacted body SOI devices and with floating body devices. In these simulations, the extra capacitance associated with the body contact is not included to show only the benefit of reduced body effect in the floating body devices. The critical path of the 64b adder consists of 21 serially-connected nMOS transistors. The addition times are estimated using an output offset voltage of 100mV – the signal required by the flip-flop. The floating body improves the critical path delay from 13% at $V_{DD}=1.3V$ to 24% at $V_{DD}=0.9V$.

The history effect in SOI – the change in delay due to previous circuit activity – is minimized by the LSCR structure, because the nMOS pass transistor network is equalized every clock cycle. During equalization, body voltage of the pass-transistors resets to the voltage at the previous equalization state. Simulation of the critical path delay through the 4b floating body adder module with for 1000 cycles at 500MHz confirm that the delay fluctuation is <0.2%.

Performance of the adder is compared with conventional CMOS adders and with a low-swing dynamic differential adder. The delay, power, and area of each adder are compared in a 32b configuration. This is because the LSCR adder, with bit length longer than 32, requires a multiple carry scheme to remain competitive. The comparison adders chosen are (1) conventional CMOS serially connected CLA adder, (2) conventional CMOS multi-level CLA adder and (3) low swing adder with dynamic driver circuit (LSDD) [1]. In the serial CLA adder, eight 4b CLA modules are connected serially. The multi-level CLA adder is a two-level CLA with four 8b CLAs in the first level and a group generate-propagate second level. The critical path through each adder is simulated with the same 0.08 μ m SOI CMOS SPICE model, and the results are plotted against supply voltage in Figure 20.2.6a. The low swing adders (LSDD and LSCR) have similar performance with the multi-level CLA (Figure 20.2.6a). However, low swing adders consume about 50% less power than the multi-level CLA adder with random inputs (Figure 20.2.6b). The power consumption of the LSCR adder is 49% lower and the delay is 8% faster than the multi-level CLA adder at 1.3V V_{DD} . Thus, the LSCR adder shows 53% better power-delay product performance compared with the multi-level CLA adder (Figure 20.2.7). Compared with the LSDD adder, the LSCR adder delay is almost the same, but power consumption is 10% lower due to the charge-recycling feature. Itemized power consumption in these adders shows more than half of the power is consumed in the full swing circuits in both the LSDD and the LSCR adders, and charge-recycling power reduction is 24% (less than the theoretical maximum 50%.) primarily due to transient leakage current during the clock transition.

References:

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- [2] H. Yamauchi et al., "An Asymptotically Zero Power Charge-Recycling Bus Architecture for Battery-Operated Ultrahigh Data Rate ULSIs," *IEEE J. Solid-State Circ.*, vol. 30, no. 4, pp. 423-431, Apr. 1995.
- [3] T. Kobayashi et al., "A current-controlled latch sense amplifier and a static power-saving input buffer for low-power architecture," *IEEE J. Solid-State Circ.*, vol. 28, no. 4, pp. 523-527, Apr. 1993.
- [4] T. Sato et al., "An 8.5-ns 112-b transmission gate adder with a conflict-free bypass-transistor logic circuits," *IEEE J. Solid-State Cir.*, vol. 27, no. 4, pp. 657-659, Apr. 1992.

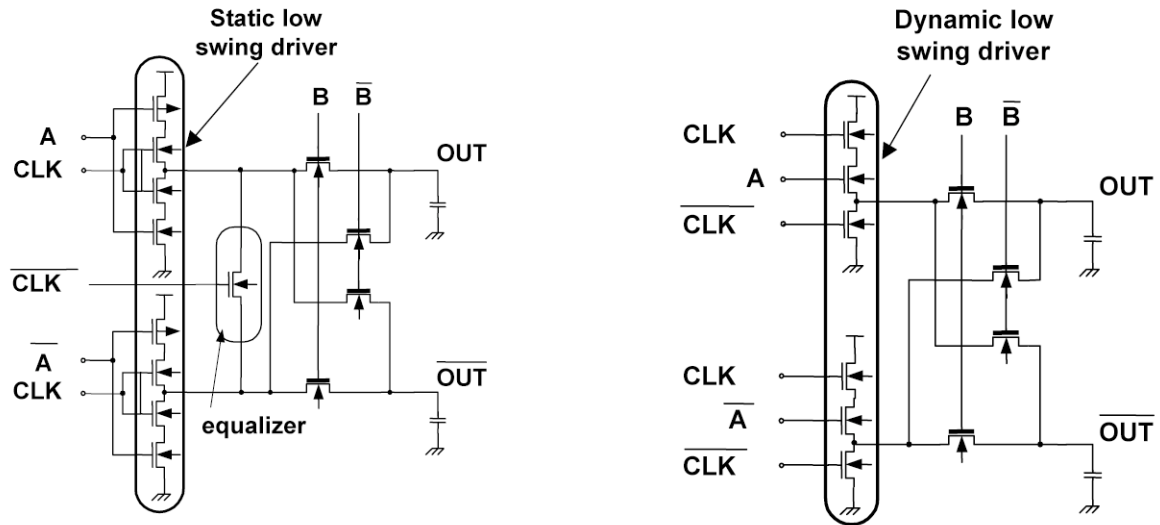


Figure 20.2.1: (a) XOR gate configuration using LSCR structure. (b) XOR gate using dynamic low swing drivers. (Previous work [1]).

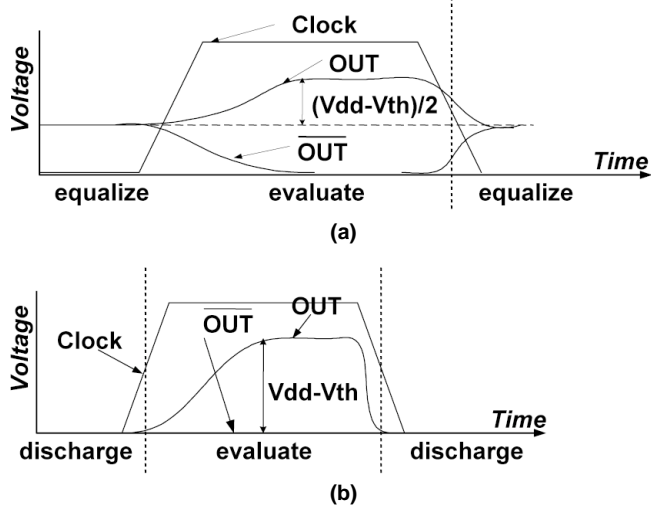


Figure 20.2.2: (a) Timing diagram of this work. (b) Timing diagram of the previous work.

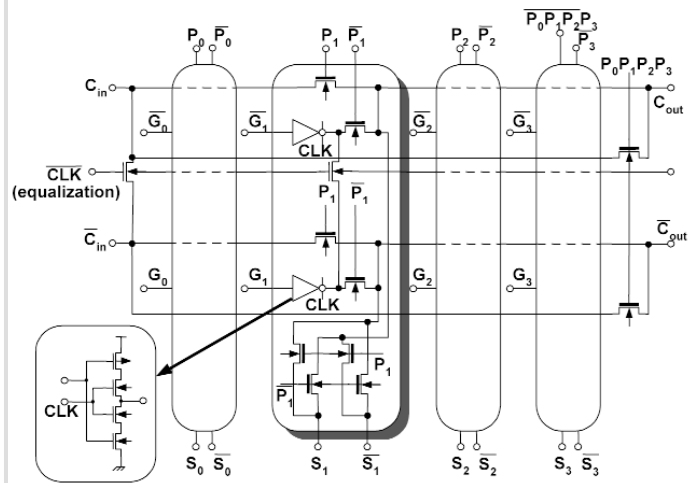


Figure 20.2.3: Four bit carry skip adder implementation using the LSCR scheme.

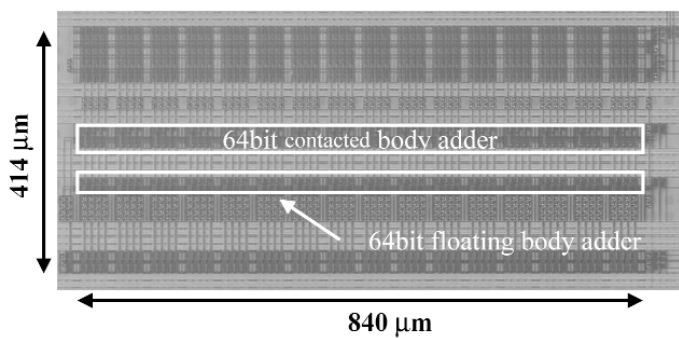


Figure 20.2.4: Micrograph of test circuit with 0.08μm SOI technology.

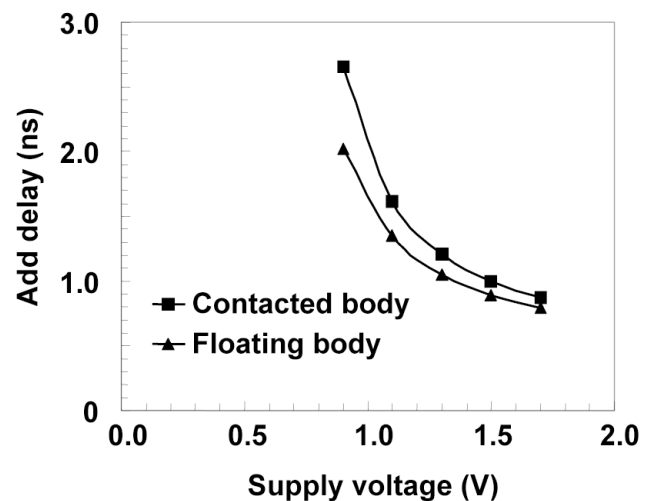


Figure 20.2.5: 64b adder delay for floating body and contacted body devices.

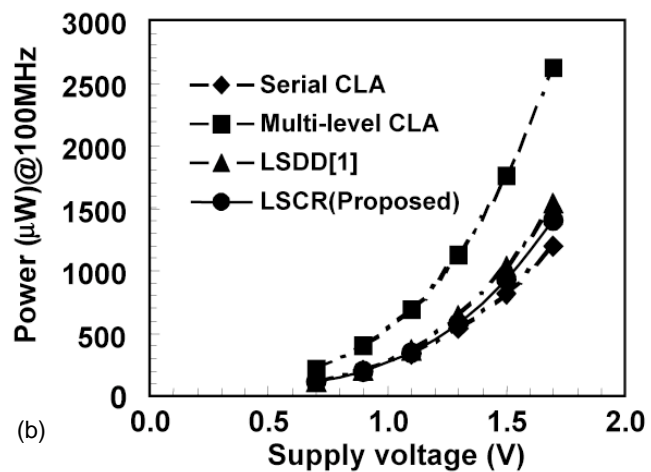
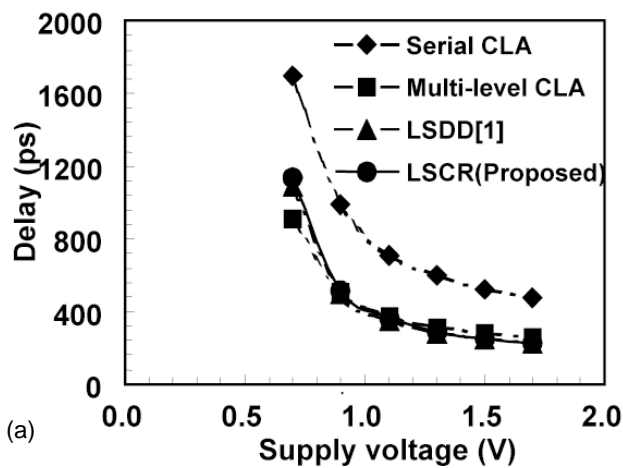


Figure 20.2.6: (a) 32b adder delay comparison with conventional adders. (b) 32b adder power consumption comparison with conventional adders.

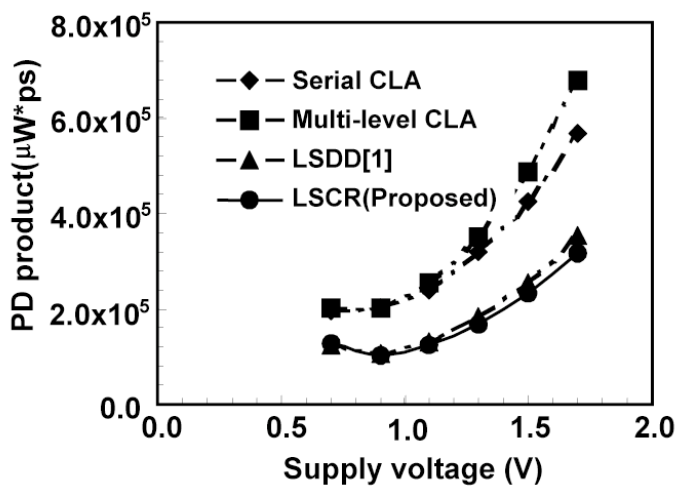


Figure 20.2.7: Power-delay product comparison with conventional adders.

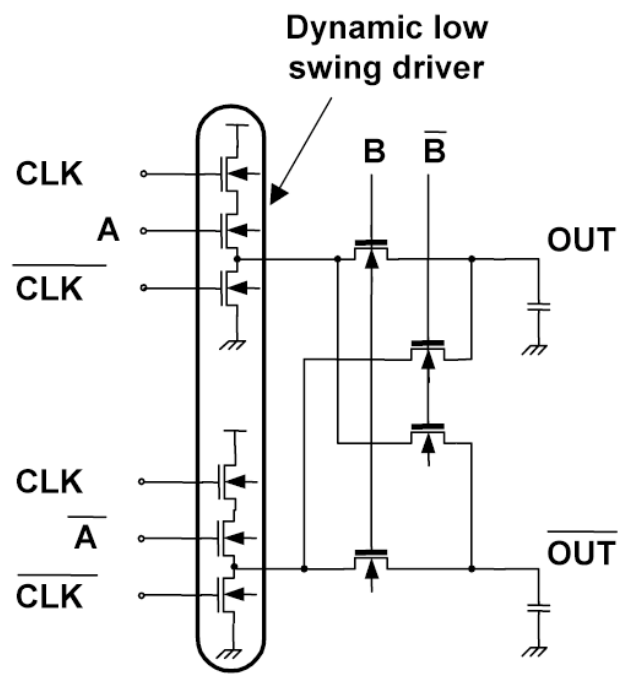
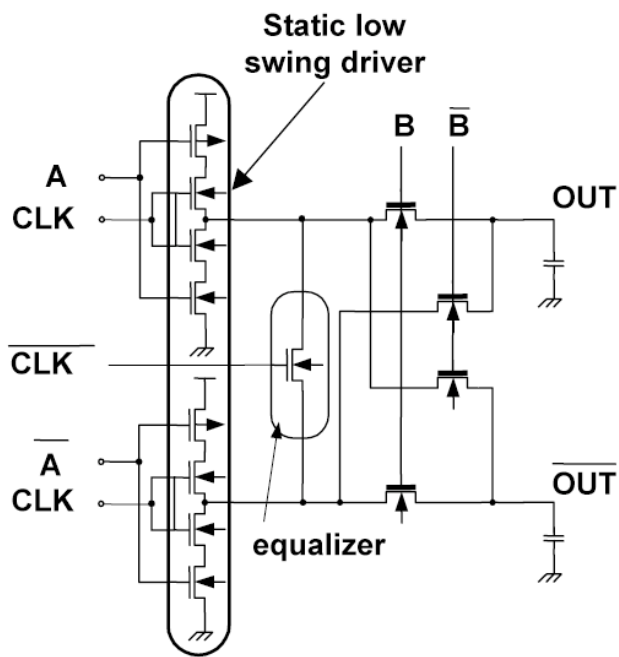


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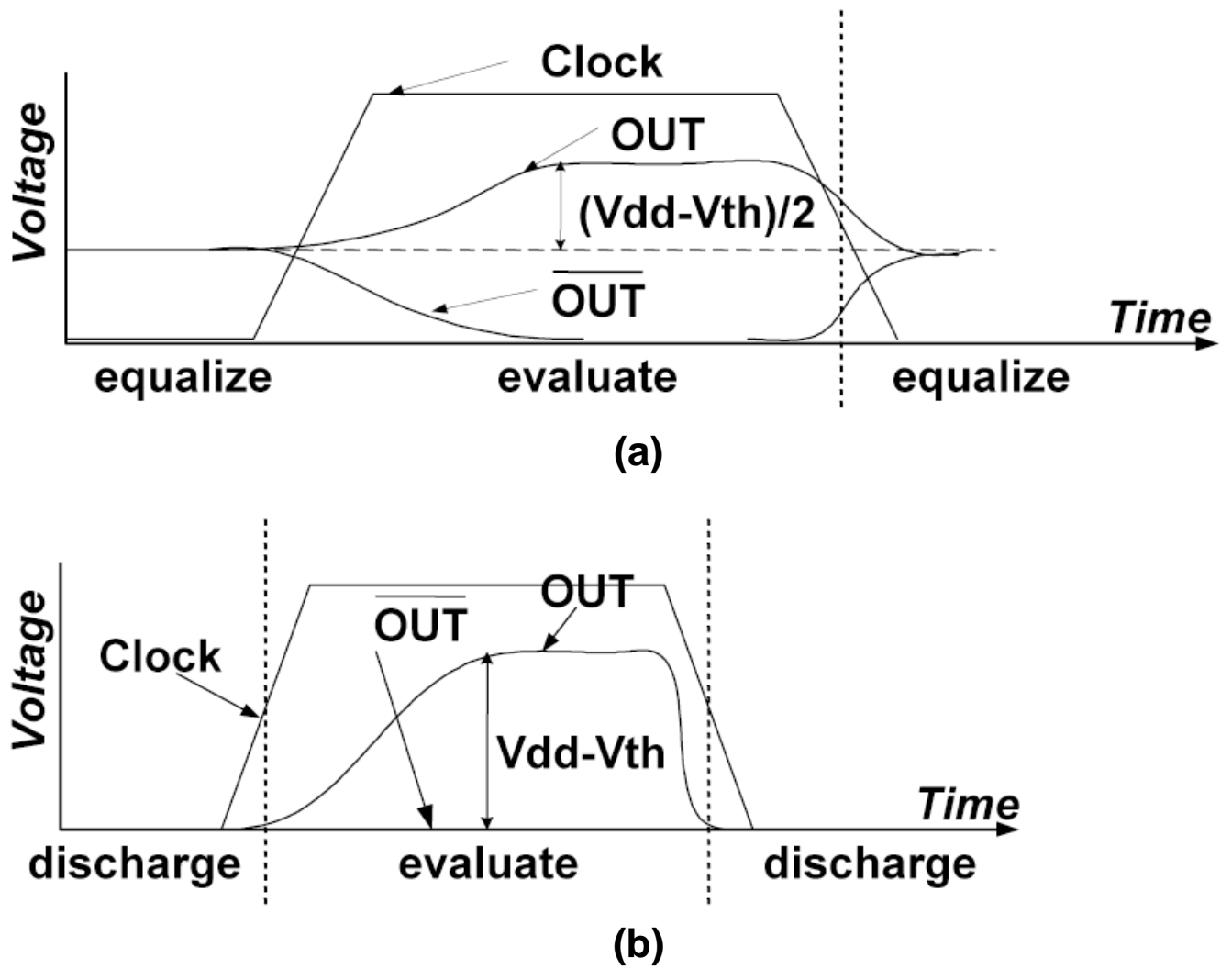


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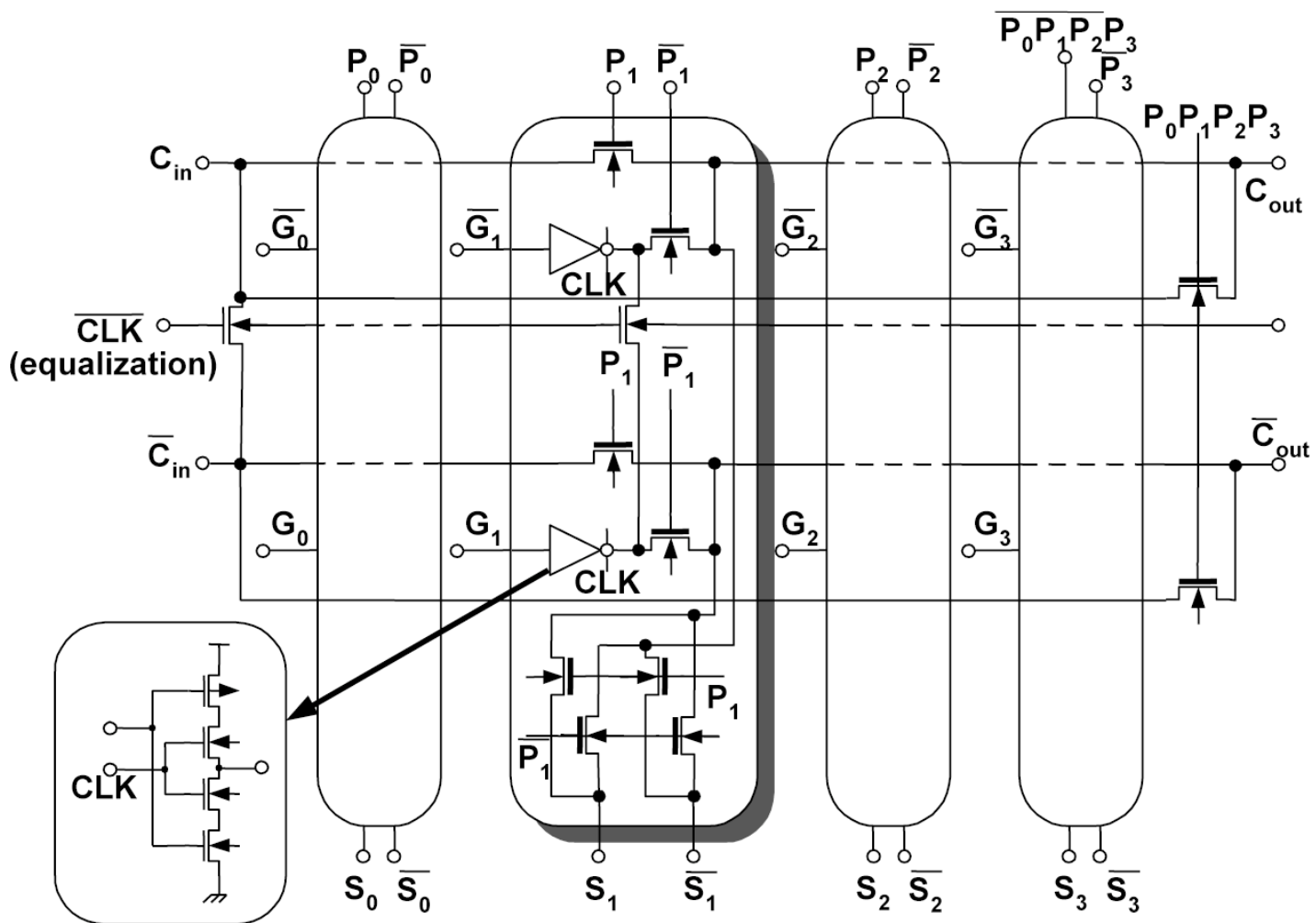


Figure 20.2.3: Four bit carry skip adder implementation using the LSCR scheme.

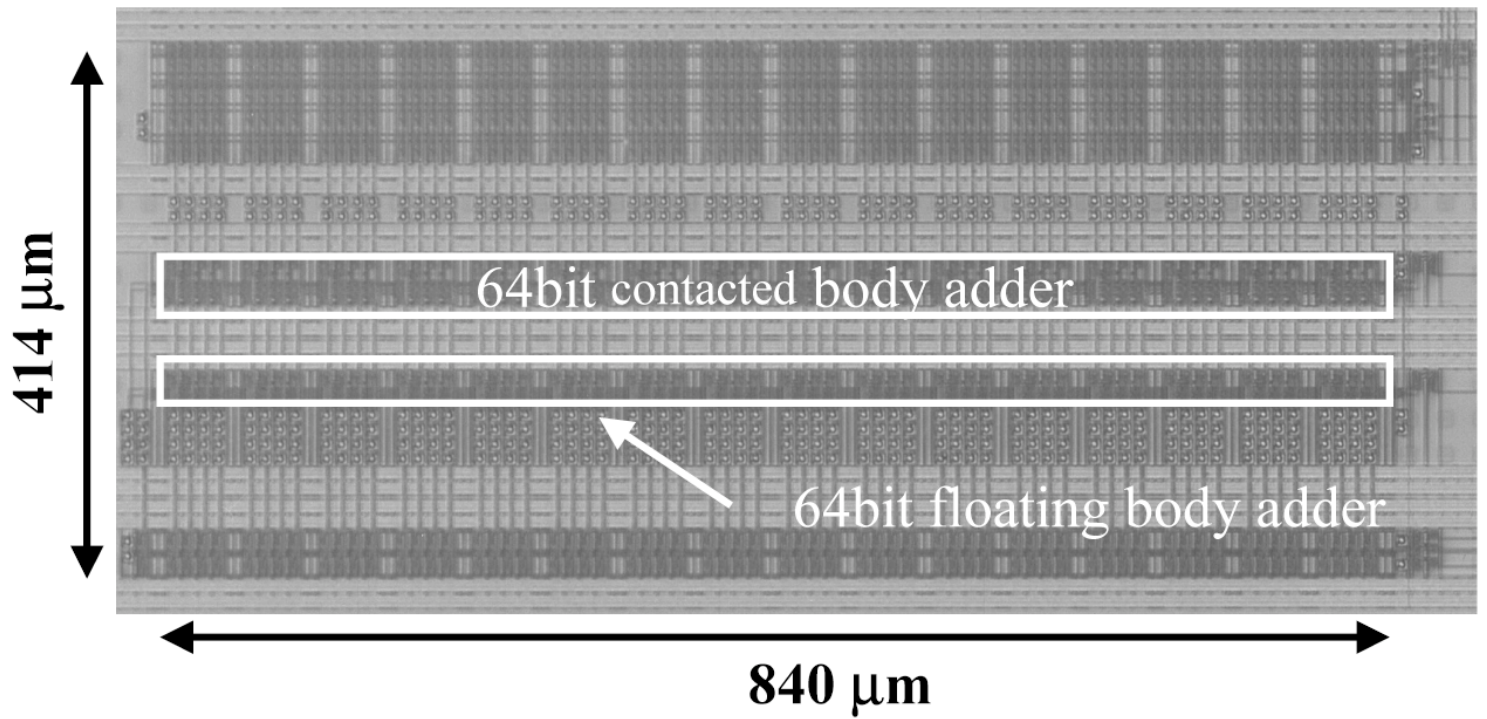


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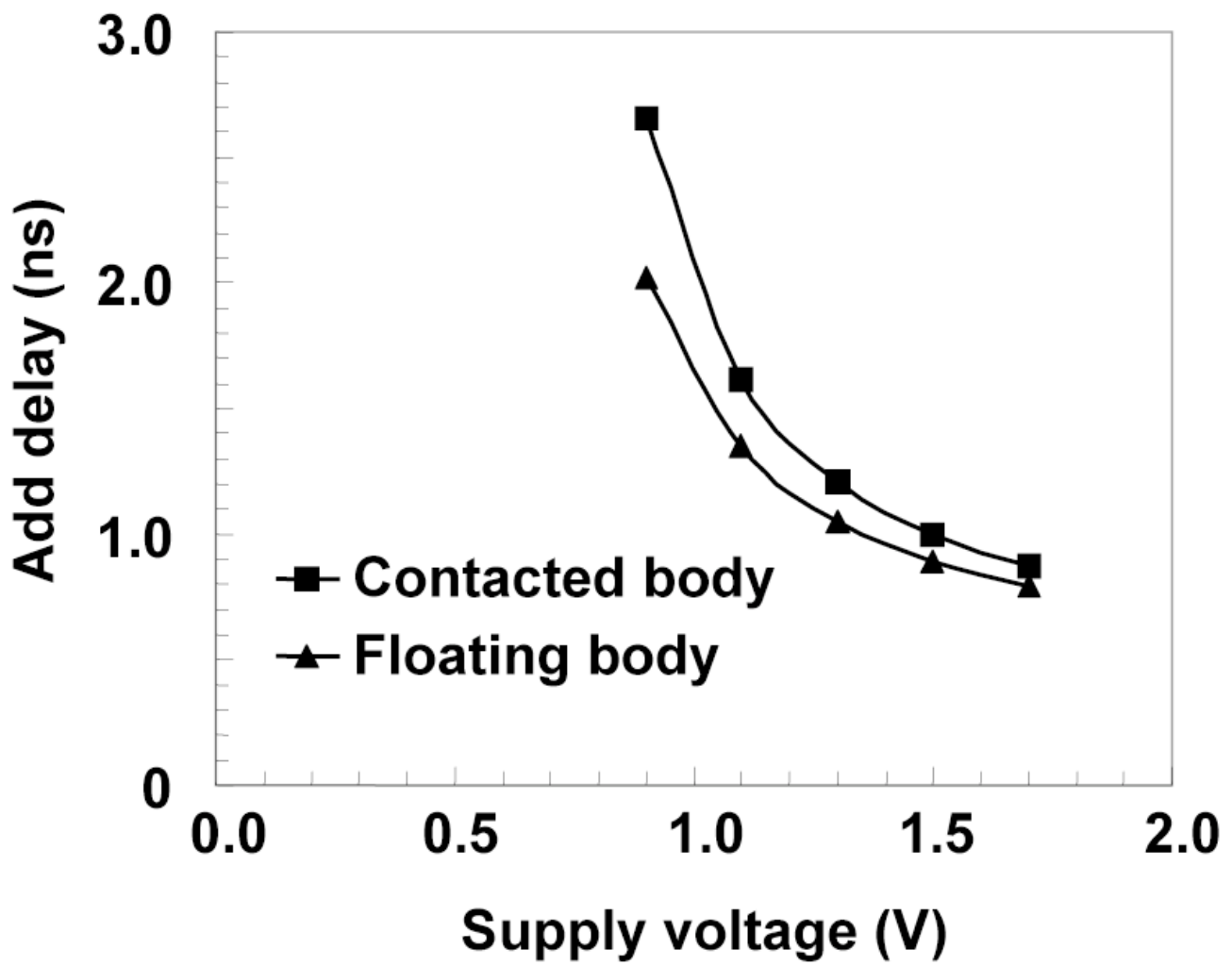


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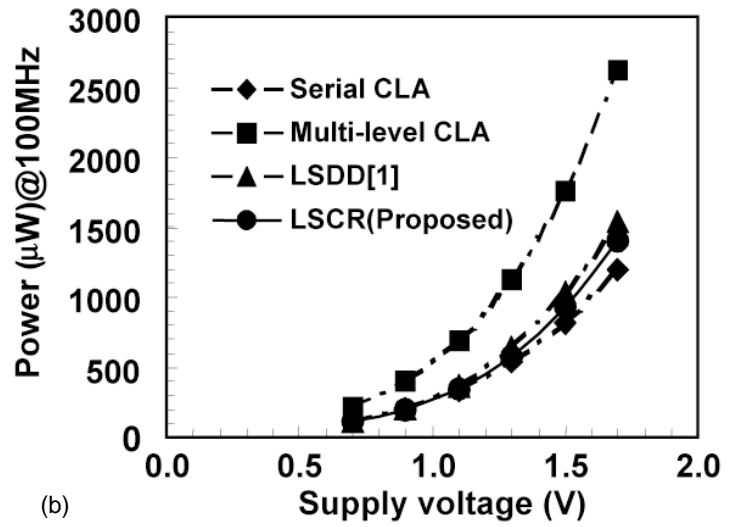
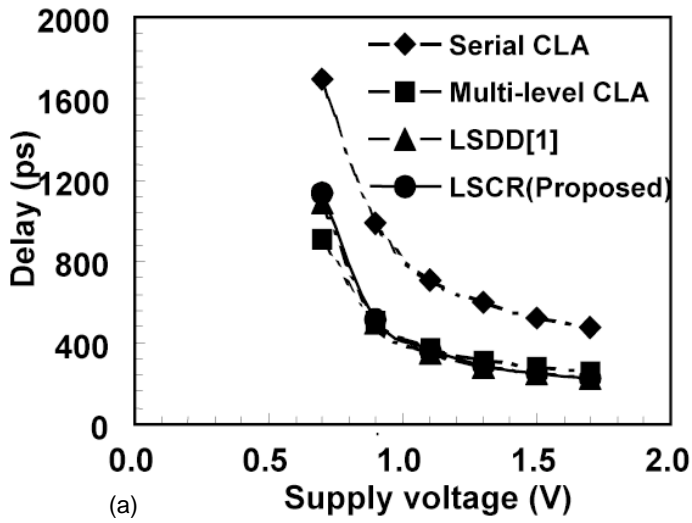


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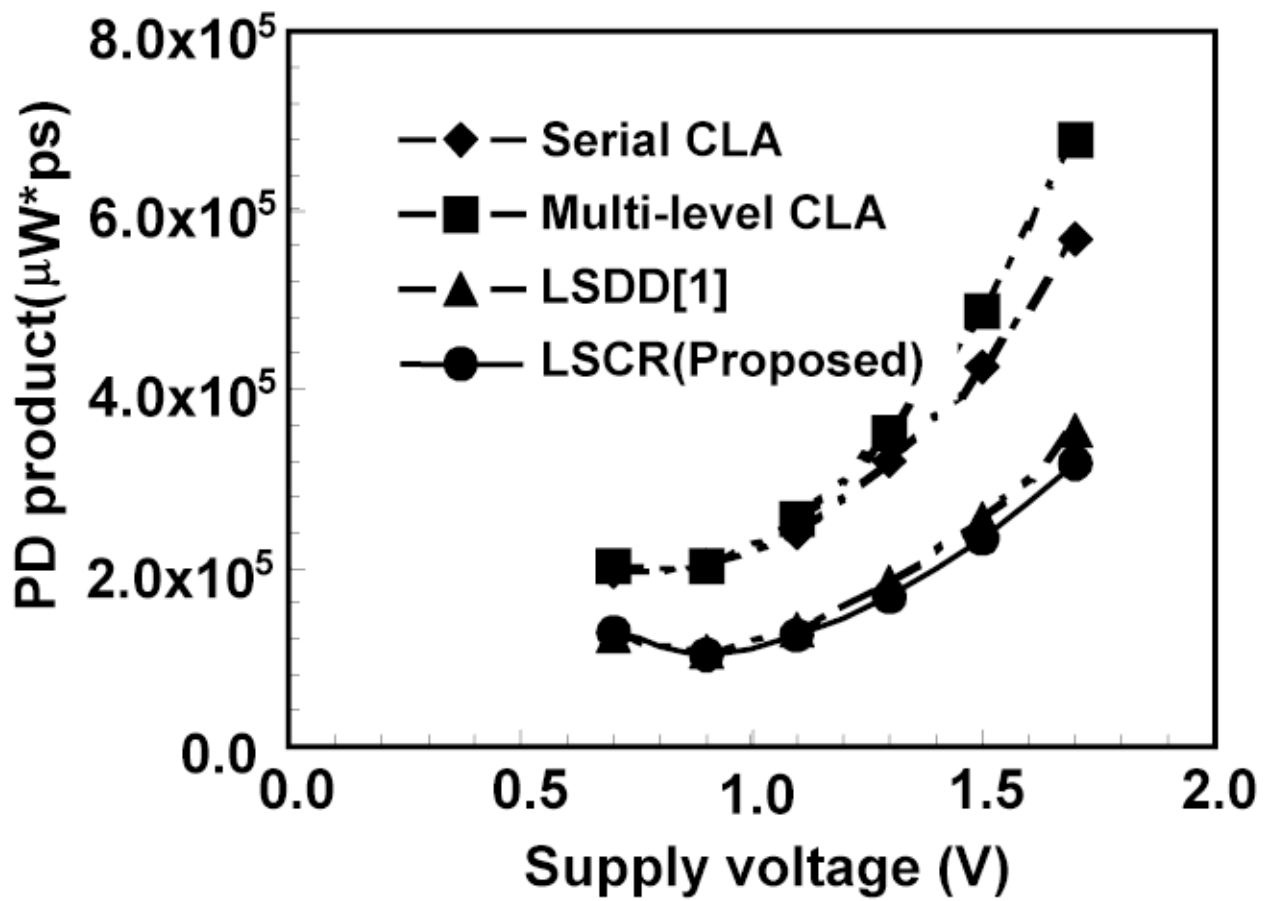


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