Dynamic Flip-Flop with Improved Power

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Abstract

An improved design of a dynamic flip-flop is presented. Proposed design overcomes the problem of the glitch at the output and improves Power-Delay Product for about 27%, while preserving logic embedding property. This is accomplished by equalizing the t_{pLH} and t_{pHL} of the flip-flop and careful design of keeper elements in the circuit. New design introduces insignificant area increase.

1. Introduction

Semi-Dynamic Flip-Flop [1] is one of high-performance flip-flops based on hybrid concept. It is used because of its small delay, logic embedding feature, size and simple topology. It is considered to be one of fastest flip-flops today (results of a recent comparison of Flip-Flop and Latches [3] are shown in Fig. 1). However, SDFF is not suitable for applications where low power is required since its power consumption limits its utilization. It is noticed that considerable portion of power dissipated in SDFF occurs due to unnecessary and false transitions that result in glitches generally increasing the power consumed by consecutive logic as well.

The paper is organized as follows. Section 2 provides background on principle of operation and limitations of Semi-Dynamic Flip-Flop. Section 3 describes improvements proposed in the paper. Section 4 presents the results obtained. Section 5 concludes the paper.

2. SDFF operation

SDFF operation falls into the category of pulsed hybrid latch approach introduced by Partovi [2]. The locking mechanism defines short period of time following active clock edge during which a change is allowed. Flip-flop is transparent during time window determined by the delay through two inverters and NAND gate (Fig. 2.). If input is at high logic level during that period, internal signal X will fall, which forces output to high level. If the flip-flop input is zero during the transparency time, there will be no other opportunity for internal signal to fall, and high level is used to force the output to low level. This mechanism ensures much smaller delay of the device for low than that for high logic level. In fact, this topology achieves proper operation using only nMOS transistors for time-critical transitions, having its origin in asymmetry between available current in nMOS and pMOS transistors. Namely, low-to-high transition is realized using intermediate inverting node (X), while high-to-low transition is done directly and thus stack of pMOS transistors is avoided. However this feature causes a "static-one-hazard" at the output when both D and Q are ones, which is a major problem of this topology. This glitch results also in unnecessary additional power consumption.

Another important issue is the use of the keepers. The keeper is used to hold the value of a dynamic node that would otherwise be in high impedance and therefore sensitive to leakage current effects and noise, especially in low-power applications where clock gating techniques are usually employed. This simple method has some disadvantages as well: in order to change the state of SDFF, two keepers have to be overpowered, which introduces another portion of unnecessary power consumption and increase in the delay. This is particularly true for the keeper at the output since in some cases, such as pass-transistor logic driven by flip-flop, it has to have certain minimal driving capability.

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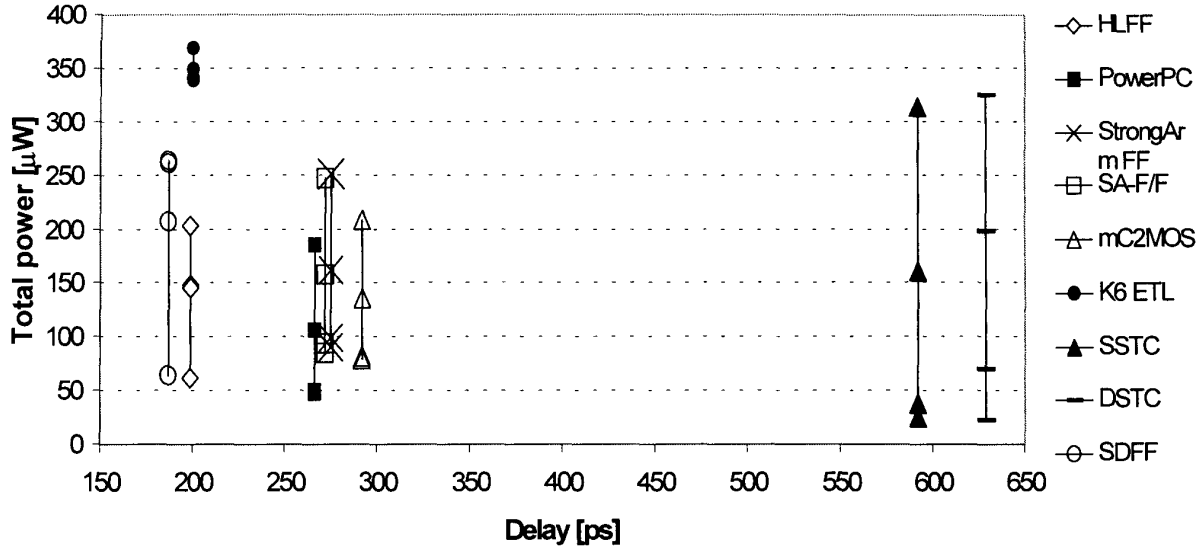


Fig. 1. Total power vs. delay for some commonly used latches and flip-flops [3]

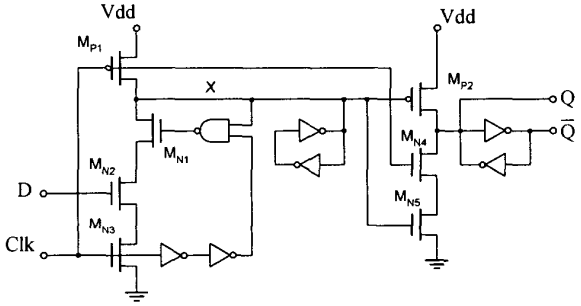


Fig. 2. Semi-Dynamic Flip-Flop

3. Improvements and optimization

Conditional capture techniques can generally be utilized if the goal is to minimize the power consumption. The idea of the conditional capture is to inhibit the transition of internal signal if this is not needed, i.e. if the output is already at the level that is to be set by the input signal. Unfortunately, application of this approach in SDFF topology requires excessive hardware overhead in the second stage, which would consume the power saved. Moreover, this requires including input D into the second stage, which seriously degrades highly desirable logic embedding property of SDFF.

Another approach is to allow transitions on internal signal but disable its effect on the output until the correct value is set. This can be accomplished by delaying the control signal for resetting the output (Fig. 3). The sizes of the transistors that equalize high-to-low and low-to-high delays are chosen.

Considering the minimization of negative effect of keepers, careful analysis shows that both low-to-high and high-to-low transitions clash can be avoided. Internal signal (X) needs to be restored only if clock is at the high logic level, and use of delayed clock for activation of the keeper allows setting the value of internal signal when keeper is inactive. In contrast, output keeper should turn on only when the clock is on low level, which is accomplished by proper selection of delayed clock signals for tri-state control of the keeper.

Another interesting observation is made, which is related to NAND gate used to ensure proper and fast transition of internal signal after clock edge. Careful analysis shows that the only purpose of the NAND gate is to allow internal node X to continue discharging after the transparency period is over. Although this can be performed by the keeper, its is not large enough (which is set by other requirements) to quickly discharge large parasitic capacitance. Use of alternative keeper structure completely eliminates the need for this NAND gate, reducing the total parasitic capacitance on critical node X.

This design requires active levels of the control signals (high level on X and delayed clock) not to overlap unless needed by functionality. There is a possible hazardous situation that should be discussed: after the clock makes transition to zero, it is not clear which of control signals of second stage will first change its state and,

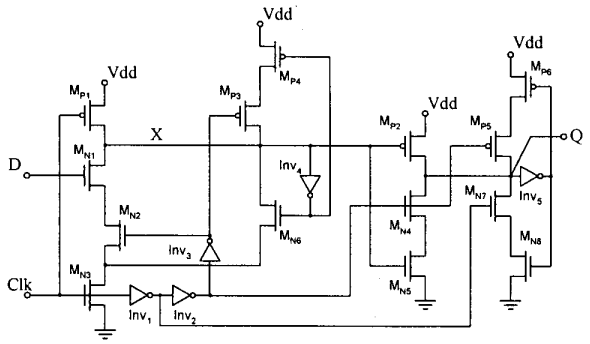


Fig. 3. Proposed flip-flop

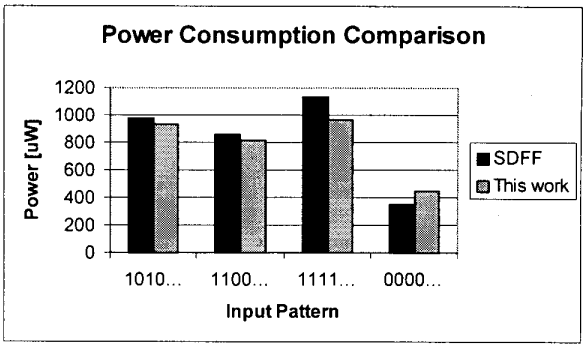


Fig. 5. Power consumption comparison

theoretically, there is a possibility that output Q be for a short time erroneously connected to ground. However, the only transistor that drives internal signal is M_{P1}, which is small, owing to the fact that there is no keeper on the node and that the capacitance on the node X is considerable, that delay is much bigger than the two inverters delay: and there presenting no danger for the proper operation of the flip-flop.

4. Results

Proposed flip-flop is simulated, optimized and compared to SDFF using 0.25μ *Leff* CMOS technology with the supply voltage of 2.5V and the load of 14 minimal inverters in the same technology. Clock frequency used for simulations is 500MHz. Transistors are sized using the algorithm presented in [3]. In addition to removing unwanted glitch at the output that could impair the performance of consecutive logic and introducing the keeper that can serve as a strong driving circuit, this flip-flop exhibits about 27% better performance in terms of PDP and about 22% in terms of delay at the negligible expense in number of transistors and area compared to SDFF.

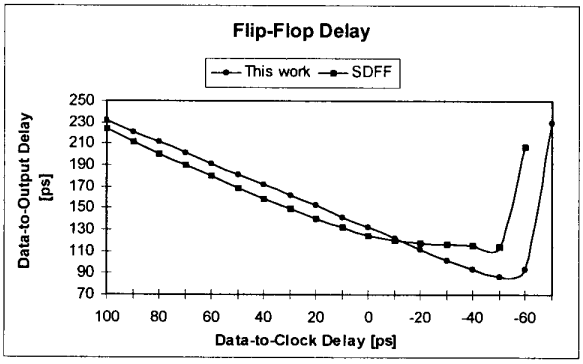


Fig. 4. Delay comparison

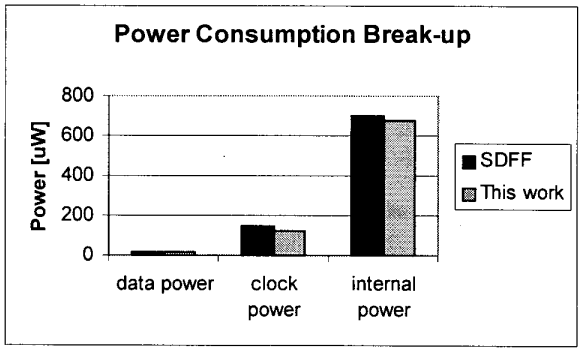
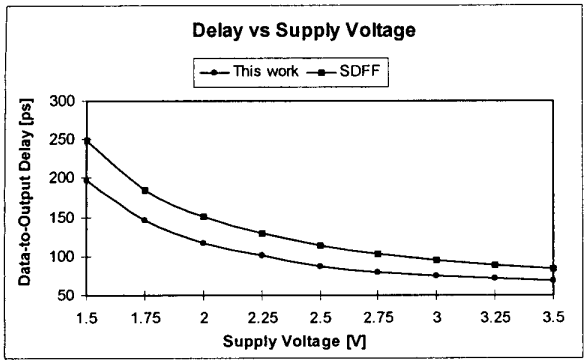


Fig. 6. Power consumption break-up

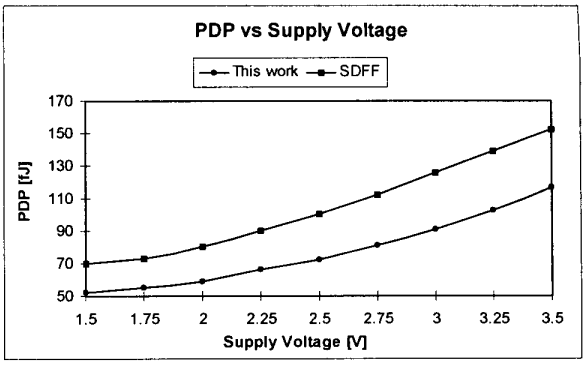
Delay characteristics are shown in Figure 4, and power consumption comparison is shown in Figures 5 and 6. It is apparent that biggest saving in power occurs when input is on the high level most of the time, which is expected from the modification description from Section 3. It can also be noticed that for comparable power consumption (which implies comparable transistor sizes), total data-to-output delay of new flip-flop is about 22% less than that of SDFF. Sizing of the transistors can be used to trade further decrease of power for speed gain obtained.

Bigger delay in stable zone ($t_{D\text{-}CLK}$ greater than zero in Figure 6) is a side effect of increased clock-to-output time for high-to-low transition, in order to minimize power consumption associated with the false transition at the output. Having no effect on flip-flop top performance, this delay can be neglected.

Fig. 7 shows behavior of both proposed flip-flop and SDFF when the supply voltage is scaled down. Although flip-flop optimization is undertaken with VDD=2.5V and results are not optimal for considerably different voltage supply, an insight into the relations can be obtained.



a) Delay vs supply voltage



b) PDP vs supply voltage

Figure 7. Performance of flip-flops with scaled voltage supply

Table 1. Summary of flip-flop characteristics

	Data-to-output delay [ps]	Average power [uW]	PDP [fJ]	Clock-to-output delay [ps]	Total transistor size [um]	Clock load [um]
SDFF	114	861	98.2	114	137.75	38
Modif. SDFF	87.4	816	71.3	130	141.25	33

5. Conclusion

Improved design of Semi-Dynamic Flip-Flop is presented. The improvements are related to the design of conditional keeping elements and delayed resetting of the output to avoid the glitch contributing power consumption. It is shown that unconditional keepers used in SDFF, although small, affect flip-flop performance both in terms of speed and power. Results showing devices' characteristics with scaling of the supply voltage are presented.

6. References

[1] F. Klass, "Semi-Dynamic and Dynamic Flip-Flops with Embedded Logic," Symp. on VLSI Circ, Digest of Technical Papers, June 1998

[2] H. Partovi, et. al., "Flow-Through Latch and Edge-Triggered Flip-Flop Hybrid Elements," ISSCC Digest of Technical Papers, pp. 132-139, February 1996

[3] V. Stojanovic, V. G. Oklobdzija, "Comparative Analysis of Master-Slave Latches and Flip-Flops for High-Performance and Low-Power Systems ", IEEE Journal of Solid-State Circuits, Vol.34, No.4, pp.536-548, April 1999.