## Designers' Notebook

## Up/Down Display Counter Counts Over Pos/Neg Range

Some applications keep track of the coordinates while moving an object stepwise in both directions. Sometimes it is desirable to display the coordinates as positive and negative numbers keeping the origin at (0,0) location. In these cases, the display counters are the part of the system that moves a silicon wafer on the probe station under control of a computer. To load any value to the displays in parallel from the computer, and for the displays to update them-

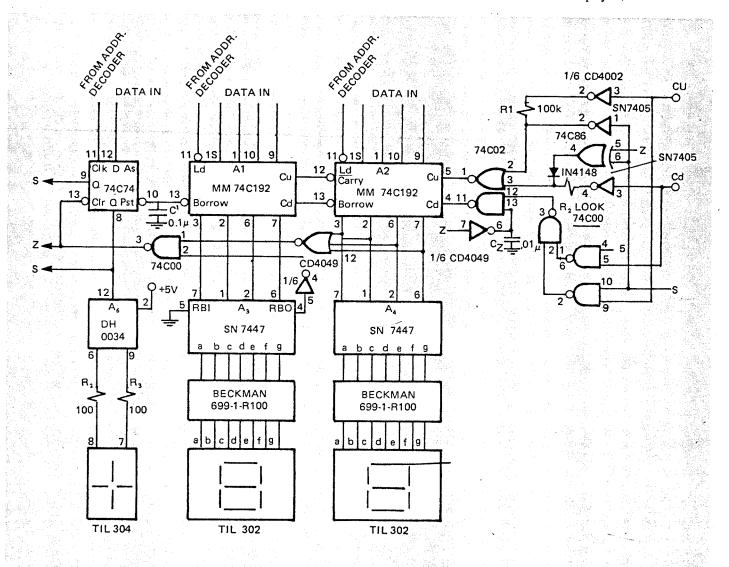
selves after any moving was received:

The counter should count up or down in response to the MOVE-UP (MU) or MOVE-DOWN (MD) pulses, depending on the number being currently displayed. If the current display is a positive number, MOVE-UP should increment the display while MOVE-DOWN should decrement it. If the number displayed is negative, MOVE-UP should decrement the display and MOVE-DOWN should increment it. Zero displayed is negative.

play is associated with the positive sign.

If MOVE-DOWN, MD, pulse is applied starting from the positive number displayed, the counter should decrement its count, change the sign to negative (after passing through zero), and continue incrementing while retaining the negative sign.

When MOVE-UP, MU, pulse is applied starting from the state when negative number is displayed, counter should



be decrementing the display, change the sign to positive when reaching zero, and continue incrementing while retaining the positive sign.

Only half, the display counter is shown; the section which displays the other coordinate is identical.

The indication of zero, Z, is derived from the units counter and rippleblanking output, Pin4, RBO, from A3, SN7447 (BCD-7 seg. decoder). The Dtype flip-flop A5 holds the sign bit, S, which is taken from the Q output. If the number displayed is negative, Q=1. Capacitors C1 and C2 serve the purpose of assuring a smooth transition from +0 to -1. The rest of the logic circuitry decides to which counter input, increment (5) or decrement (4), to direct the moving pulse, depending on the number currently being displayed, S and Z status, and the move pulse applied, MU or MD.

The circuit is not intended to operate at high rates, but its response is smooth until the rate of 10 KHz, and it responds to the one-to-zero-going pulses greater than  $2 \mu S$ .

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## Debugging Via ROM Breakpoint

It is often necessary to gain access to address and register contents of ROM resident firmware during debugging or maintenance. In RAM-resident-systems, this is easily handled by available debugging software or simple instruction substitution at a suspect address. However, when a firmware controlled system has a hanging loop of unknown address or some other malfunction which requires register or RAM examination, this logic analyzer approach proves useful. The primary requirements for this technique are a logic analyzer with capacity for decoding the address/data bus in use and a trigger word output which can be used to generate an interrupt. An interrupt handling routine (described below) must be resident in ROM.

Functionally, interrupt handling routines save registers and flags on the stack (and can also read RAM locations, if desired). The routine works as soon as an interrupt trigger is generated by an address match in the logic analyzer (the

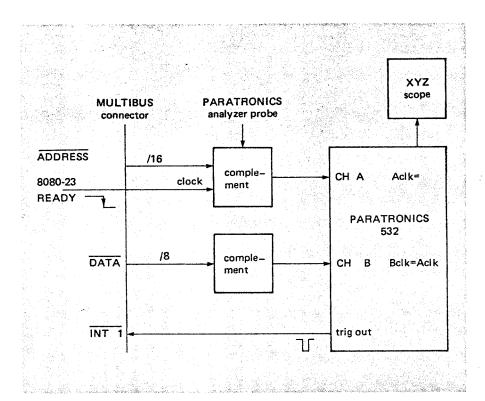


Figure 1:80/10 connections

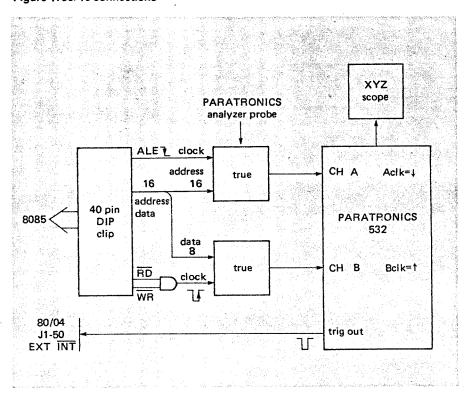


Figure 2: 80/04 connections

logic analyzer trigger word can be the "breakpoint" address or "don't care" in the case of a hung loop). The occurrence of the trigger word starts the logic analyzer address/data acquisition process. The interrupt generated by the trigger word causes a branch to the routine which puts register contents onto the bus and thus into the logic analyzer.

This technique has been employed on Intel 80/10 and 80/04 systems utilizing a Paratronics 532 logic analyzer.

The basic approach can be applied to virtually any CPU/logic analyzer combination. Figure 1 and 2 depict interconnections used with 80/10 and 80/04 systems. The logic analyzer approach (use of trigger words) is efficient in gaining access to address and register contents.

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