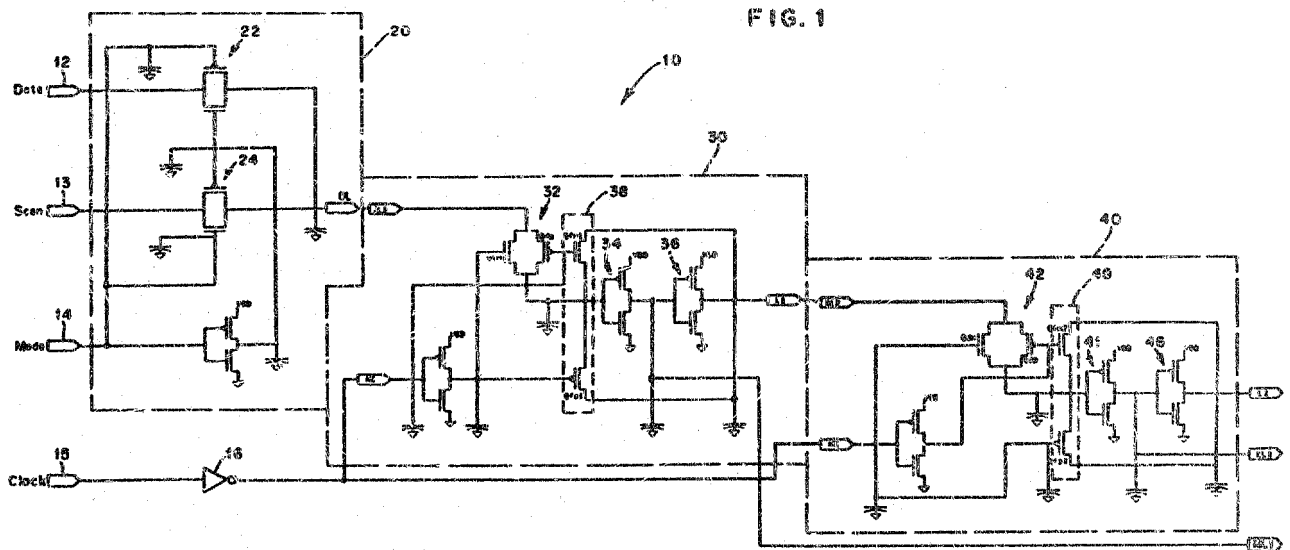


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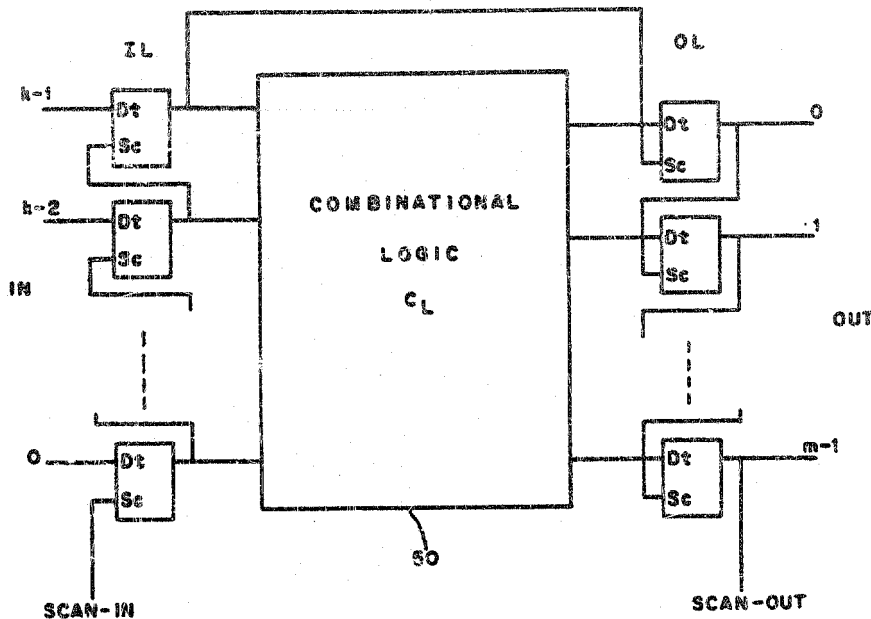
SINGLE CLOCK CMOS LATCH COMPATIBLE WITH LEVEL-SENSITIVE SCAN DESIGN



A single clock CMOS latch for level-sensitive scan design (LSSD) compatibility is provided and comprises an input switch, a master stage and a slave stage. The timing and operation of the switch and stages is such that when the clock is active, the master stage is decoupled from the slave stage, new data is gated into the master, and a feedback path is enabled in the slave stage to hold the latch state. When the clock is inactive, a feedback path in the master stage is enabled, the feedback path in the slave is disabled, and new data proceeds to the output of the slave stage. The provided latch is free of races and provides LSSD compatibility. The provided latch is advantageous as opposed to the LSSD compatible latches of the prior art as the latches of the prior art require the use of two non-overlapping clocks.

The preferred single clock LSSD compatible CMOS latch is seen in Fig. 1. The latch 10 incorporates as inputs a normal data input 12, a scan data input 13, a mode input 14, and a single clock input 15 which is inverted by inverter 16 and supplied as a "not" clock input NC to the stages 30 and 40. The latch 10 is seen to comprise an input switch 20, a master stage 30 and a slave stage 40, with device ratios being those preferable for circuit simulation arrangements. The outputs of the latch include both polarities of the slave stage 40, as well as the negative polarity of the master stage 30.

FIG. 2



Input switch 20 is essentially comprised of two pass-switches 22 and 24 multiplexed together under the control of the mode input 14. Each pass-switch is enabled by one level of the mode input to allow either the data at the data input 12 or the scan input 14 to proceed to the output DL in a mutually exclusive fashion. If desired, additional data inputs to the latch could be utilized provided that an additional pass-switch was added per data input and provided that appropriate control lines were added.

Master stage 30 essentially comprises an input pass-switch 32 which is under control of the clock input NC, an inverter pair 34, 36 connected in series which has the output of the pass-switch 32 as an input and a feedback path via pass-switch 38 also connected to its input. As shown, pass-switches 32 and 38 are activated by opposite levels of the clock input. In operation, when the clock is low (NC is high), data at IL1 is prevented from latching since pass-switch 32 is turned off. The feedback path from the output of 36 to the input of 34 is enabled, however, as pass-switch 38 is turned on. When the clock rises, NC falls, and the feedback pass-switch 38 is deactivated while the input pass-switch 32 is activated. After the delay time through the input pass-switch and the inverters 34 and 36, data at IL1 is valid at the output L1 of the master stage 30. When the clock falls again, the feedback pass-switch 38 is again enabled and the input pass-switch 32 is again disabled.

The slave stage 40 is schematically equivalent to the master stage 30 except that the input and feedback pass-switch 42 and 48 are fed by the opposite polarity of the clock input. Thus, when the clock is low and NC is high, the output of the L1 latch is present at IL2, the input pass-switch 42 is enabled, the feedback pass-switch 48 is disabled, and the positive and negative latch outputs are available at L2 and NL2. When the clock rises, the feedback pass-switch 48 is enabled, activating the latching of the previous data in L2, while the input pass-switch 42 is disabled. During this time, data is propagating through the master stage 30 and the master latch drives data through the slave latch. Since the input pass-switch 42 of the slave latch is level-sensitive, data cannot pass from the master through the slave to effect a race in the system.

The operation of the latch 10 during scan mode is understood with reference to Fig. 2 which illustrates a combinational logic network 50 having k inputs and m outputs. The inputs are taken from k input latches IL and the outputs are fed into the data input of m latches OL at the output. All the input latches are connected together in a k+m long LSSD chain. The output latches are likewise connected. The procedure for testing combinational logic 50 comprises:

1. Set MODE to high logic level.
2. Advance clock k cycle (scan test vector into input latches).
3. Set MODE to low level (normal operation).
4. Advance clock one cycle to perform logic operation on test vector and latch result into output latches.
5. Change MODE to high level.
6. Advance clock for k+m cycles such that the result of the operation on the test vector is scanned out from the output latches, and scan new test vector into input latches.
7. Go to step 3.

With the provided latch circuitry, it will be appreciated that various timing and clocking considerations must be taken into account. Thus, for example, the clock pulse width must be greater than or equal to twice the inverter delay time (T_{inv}) plus twice the delay of the input switch stage 10 (T_{sw}). Also, the maximum amount of time allowed for logic operations must be less than or equal to the total cycle time minus $4T_{inv}$ minus $3T_{sw}$ minus the fall time of the clock signal minus twice the clock skew time. Other timing considerations required for the optimal operation of the provided CMOS latch will be appreciated by those skilled in the art.